CERTAIN INVESTIGATIONS ON DUAL EDGE TRIGGERED SENSE AMPLIFIER FLIP-FLOPS FOR LOW POWER AND HIGH PERFORMANCE APPLICATIONS

A THESIS

Submitted by

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CERTIFICATE

This is to certify that all corrections and suggestions pointed out by the Indian /Foreign Examiner(s) are incorporated in the Thesis titled " Certain Investigations on Dual Edge Triggered Sense Amplifier Flip-Flops for Low power and High performance applications " submitted by Mr. Mahendrakan.K

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Proceedings of the Ph.D. Viva-Voce Examination of Mr.Mahendrakan.K held at 10.00 AM on 26.02.2020 in Conference hall,NEC Department of Electronics and Communication, Nandha Engineering College, Erode.

The Ph.D. Viva-Voce Examination of Mr.Mahendrakan.K (Reg. No. 1213469785) on his/her Ph.D. Thesis Entitled " Certain Investigations on Dual Edge Triggered Sense Amplifier Flip-Flops for Low power and High performance applications " was conducted on **26.02.2020** at 10.00 AM in the Conference hall,NEC Department of Electronics and Communication, Nandha Engineering College, Erode..

The following Members of the Oral Examination Board were present:

1. Dr. Rajeev Gupta,Professor and Head,Department of Electronics and Communication Engineering,University College of Engineering Rajasthan Technical University,Kota - 324 010 Rajasthan — Indian Examiner
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The research scholar, Mr. Mahendrakan.K presented the salient features of his/her Ph.D. work. This was followed by questions from the board members. The questions raised by the Foreign and Indian Examiners were also put to the scholar. The scholar answered the questions to the full satisfaction of the board members.

The corrections suggested by the Indian/Foreign examiner have been carried out and incorporated in the Thesis before the Oral examination.

Based on the scholars research work, his/her presentation and also the clarifications and answers by the scholar to the questions, the board recommends that Mr.Mahendrakan.K be awarded Ph.D. degree in the **Faculty of Information and Communication Engineering**.

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The research work embodied in the present Thesis entitled **"CERTAIN INVESTIGATIONS ON DUAL EDGE TRIGGERED SENSE AMPLIFIER FLIP FLOPS FOR LOW POWER AND HIGH PERFORMANCE APPLICATIONS"** has been carried out in the Department of Electronics and Communication Engineering, Nandha Engineering College, Erode. The work reported herein is original and does not form part of any other thesis or dissertation on the basis of which a degree or award was conferred on an earlier occasion or to any other scholar.

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ABSTRACT

In this digital computing world Very Large-Scale Integration (VLSI) plays the major role. Recent emerging applications requires a high-performance VLSI circuits with high speed, low power consumption, reducing area usage and clock skew tolerance. One of the crucial factors in modern circuit system is reducing the power consumption. Clock trees and the Storage elements consumes more power. Major part of the total power dissipation is obtained by clock systems and the storage systems such as Flip Flops (FFs). Hence by focusing on the Flip Flops and clock systems, power consumption can be reduced and it is the main objective of this research work. According to today's power budget, portable circuits are severely restricted. It is essential to diminish the power dissipation in both Flip Flops (FFs) and clock distribution networks. For fast and high frequency operations, the Flip Flop's latency needs to be reduced. Hence recent research studies aims to provide a novel design for Flip Flops which assures less power consumption and less latency.

For reducing the power consumption in the clock distribution network, various existing techniques were reviewed which includes, the Sense Amplifier Flip Flop (SAFF), Single Edge Triggered Flip Flop (SETFF), Dual Edge Triggered Flip Flop (DETFF) and Clock Gated Sense Amplifier Flip Flop (CGSAFF). The study of existing Flip Flop architectures, initiated to propose a new Flip Flop architecture called the Modified Clock Gated Dual Edge Triggered Sense Amplified Flip-Flop (MCGDET-SAFF). The suggested MCGDET-SAFF is derived from the modification or extension of the Flip Flop models. That is, from simple Flip Flop into Sense Amplified Flip Flop, the Sense Amplified Flip Flop into Dual Edge

Triggered Flip Flop, then it will be extended into Clock Gated Dual Edge Triggered Sense Amplified Flip Flop. Finally, it is modified into MCGDET-SAFF.

From the basic design each modification provides an improvement in decreasing power consumption and increasing the speed of the application where MCGDET-SAFF is used. The altered Clock Gated Double-Edge Triggered–Sense Amplified Flip-Flop is used in this study to enhance efficiency through the reduction of energy usage. This is achieved by lowering the clock changing energy which reduces the interval and prevents energy leakage. Contrary to several previously gated FFs, MCGDET-SA FF includes holding properties to reduce consumption and alter the methods of switching circuits from inactive to active and passive to inactive. The energy dissipation is achieved by improving the response route. Fewer transistors are used to decrease the region of silicon in the current gating technique. The suggested Sense Amplified FF reduces the time and improves the velocity at which the energy usage decreases further. Also, by exhausting haste symmetrical latch, the MCGDET-SA Flip Flop is able to accomplish lower power dissipation and delay. This technique is mainly utilized to diminish the active power indulgence in synchronous circuits. The proposed design has considered the baseline circuit, which developed a novel Clock Gated FF to decrease the power dissipation further during low switching activity. Based on the analysis, Low power and High performance modified clock gated sense amplifier-based Flip Flop is proposed by integrating high speed operation, less area utilization and less power consumption from the existing designs.

The proposed Flip Flop is modelled and the outcomes are checked for different feed voltages. The proposed MCGDET-SAFF is not designed

directly from the basic Flip Flop design circuit. To obtain the final circuit with high efficiency in terms of low power and high speed, stage wise improvement is done on the Edge Triggered Flip Flop (ETFF). So at every stage the performance gets improved. This new design is established to decrease the power dissipation and delay when associated with the Clock Gated Sense Amplifier Flip-Flop (CGSAFF) up to 26.1% and 86.5% respectively. The suggested MCGDET-SAFF was designed using the CMOS 0.13μm method technologies of National Electronics Limited. From the results, the proposed MCGDET-SAFF has the lowest delay than the other Flip Flops. It has achieved 78% of the reduction in delay. Various test patterns are used for simulating the FF designs. In this research work, six models were considered under multiple situations. The test outcome demonstrates that the power usage and delay has improved when compared to the other Flip Flop frameworks.

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MAHENDRAKAN K

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LIST OF SYMBOLS AND ABBREVIATIONS

ACSAFF	-	Adaptive Clocking Dual Edge-Triggered Sense-
CDN	-	Clock Distribution Network
CG	-	Clock Gating
CG-SAFF	-	Clock Gated Sense Amplifier Flip Flop
CPL	-	Complementary Pass transistor Logic
CPS-FF	-	Clock Pair Shared Flip Flop
CPSFF-PTL	-	Clock Pair Shared Flip Flop with Pass transistor Logic
CCFF	-	Conditional Capture Flip-Flop
CDFF	-	Conditional Discharge Flip-Flop
CDMFF	-	Conditional Data Mapping Flip-Flop
CGFF	-	Clock Gated Flip-Flop
DET	-	Dual Edge Triggered
DETFF	-	Dual Edge Triggered Flip Flop
DETSAFF	-	Dual Edge triggered Sense Amplifier Flip-Flop
DET-SAFF	-	Dual Edge Triggered Sense Amplifier Flip Flop
DET SE	-	Dual-Edge Triggered Storage Elements
DE-DCCER	-	Dual-Edge Triggered Differential Conditional Capturing Energy Recovery
DIBL	-	Drain Induced Barrier Lowering
DSPFFs	-	Dual-Edge Triggered Static Pulsed Flip-Flops
DRFF	-	Data Retention Flip-Flop
ELFF	-	Embedded Logic Flip-Flop
ETFF	-	Edge Triggered Flip Flop
FF	-	Flip-Flop
EPTFF	-	Explicit Pulse Triggered Flip Flop

FPTG	-	Four-Phase Transmission Gate
HEA	-	High Efficiency Application
HLFF	-	Hybrid Latch Flip-Flop
IPTFF	-	Implicit Pulse Triggered Flip Flop
LCFF	-	Level Converting Flip-Flop
LSDFF	-	Low-Swing Clock Double-Edge Triggered Flip-Flop
LSSD	-	Level Sensitive Scan Design
MS	-	Master Slave
mC²MOS	-	Modified C²MOS Master-Slave Flip-Flop
MDETSAFF	-	Modified Dual Edge Triggered Sense Amplifier Flip-Flop
MCGDET-SAFF	-	Modified Clock Gated Dual Edge Triggered Sense
MCG-SAFF	-	Modified Clock Gated Sense Amplifier Flip Flop
PIPO	-	Parallel In – Parallel Out
PISO	-	Parallel In – Serial Out
PTL	-	Pass Transistor Logic
PG	-	Pulse Generator
PTFF	-	Pulse Triggered Flip Flop
RCSFF	-	Reduced Clock Swing Flip-Flop
SDFF	-	Semi-Dynamic Flip-Flop
SAFF	-	Sense Amplifier Flip Flop
SET SE	-	Single Edge Triggered Storage Elements
SIPO	-	Serial In – Parallel Out
SISO	-	Serial In – Serial Out
SETFFs	-	Single Edge-Triggered Flip-Flops

SCDFF	-	Static Output-Controlled Discharge Flip-Flop
TGMS	-	Transmission-Gate based Flip-Flop
TGFF	-	Transmission gate Flip-Flop
TSPC	-	True Single-Phase Clock
VLSI	-	Very Large Scale Integration

CHAPTER 1

INTRODUCTION

1.1 OBJECTIVE

This chapter presents the detailed information from the basic Flip Flop to Modified Clock Gated Sense Amplified Flip Flop. It explains about the fundamental gates that are used for arithmetic functions in the Flip Flop circuit and they can directly be integrated into any VLSI circuits used for recent electronic applications. After reading this chapter any layman can understand about Flip Flop functionalities, applications and various architectures with the applications. Also, it is very easy to understand the entire research work easily.

1.2 INTRODUCTION

One of the most important elements which can determine the power consumption in any VLSI circuits is Flip Flop. Flip Flop is one of the electronic circuits storing binary data using two different stable states. By changing the inputs different data can be stored. Latches and Flip Flops are the fundamental constituent of digital electronic systems applied in personal computers, communication systems and so on. The Flip Flops are used in various applications based on digital electronic circuits such as counters, shift registers, frequency dividers and storage registers. Making a circuit active is called as triggering. The circuit that becomes active at any state such as positive or negative of the clock signal is called Edge Triggered Flip Flop

(ETFF). The Circuit that becomes active at both positive and negative state of the clock is called Dual Edge Triggered Flip Flop (DETFF). DETFF provides high throughput and it is handy in applications. But it is important to notice that, contemporary cell libraries are not using dual edge triggered Flip Flop.

Recent emerging applications require a high-performance VLSI circuits with high speed, low power consumption, reduced area usage and clock skew tolerance. One of the crucial factors in modern circuit system is reducing the power consumption. Clock trees and the Storage elements consume more power. 30% to 60% of the total power dissipation is obtained by the clock systems and the storage systems such as Flip Flops. Hence by focusing on the Flip Flops and clock systems, power consumption can be reduced and it is the main objective of this research work. Various synchronous circuits used for reducing dynamic power dissipation mainly use clock gating technique. It is used for reducing the power consumption and saves the power. Instead of clock trees, Flip Flops are used, since they are having switching states. This research work is focused on designing and implementing an efficient modified clock gated sense amplified dual edge triggered Flip Flops to obtain low power consumption and delay.

Dual edge triggered Flip Flop is an efficient approach. There are two different kinds of Flip Flops designed as single edge and dual edge triggered Flip Flops. The storage elements of DETFF has the ability to capture the signal at both raising-edge and falling-edge of the CLK. One of the objectives is to design a short pulse close to the triggering edge and it is considered as the CLK-input to the FF. This storage element of the DETFF is incorporated into clock gating technique, where it reduces the power consumption in any idle circuit dynamically. Though, asynchronous data sampling and miscommunication problem will be created among the edges and the clock. Clock gating is applied when D=Q, since it would be

unnecessary to sample the same signal value to store into the Flip Flop. Transitions of D are used to assert the CG signal. The C is the internal clock pulse that triggers the Flip Flop. For the gating mode, the C maintains its value instead of generating an active edge. For the non-gating mode, C changes after the transition on CLK. Suppose if D changes (ie enters the non-gating mode) while C≠CLK, then an asynchronous data transition may occur that is visible on the output. Henceforth, this research work focuses on designing a dual edge triggered clock gated Flip Flop for increasing the efficiency of the digital circuit systems.

1.3 ABOUT FLIP FLOPS

The basic component of an electronic circuit with two stable-states to persist binary data (0/1) is Flip Flop. Based on the input given to Flip Flop the stored data can be changed. Latches and Flip Flops are the main element for all the digital electronic components utilized in computers and communication devices, also they are used for storing data in computing devices and it is the fundamental storage component in sequential logic. Before start learning Flip Flops, it is necessary to understand the difference between Flip Flops and latches. Latches are similar to Flip Flops, but it is different in logic.

1.3.1 Flip Flop Vs. Latches

The Flip Flop and latches are differentiated only in terms of clocking and gating method. For example, consider a SR-Latch and SR-FF, when setting S as active, the output Q is high and the output Q' is low. In SR-latch when S is set as active the output Q is low. The logic diagram of SR-Latch is depicted in Figure 1.1.

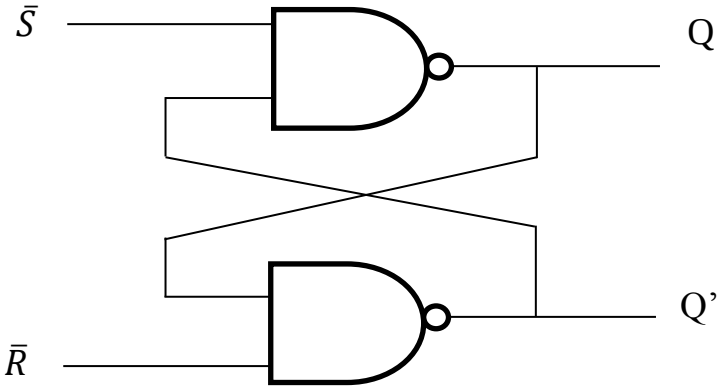


Figure 1.1 SR-LATCH

But a Flip Flop is synchronous and it is called as gate or clock method-based SR latch. In the Flip Flop circuit, the output of the stored data gets changed only when the input clock signal is active. The logic diagram of SR-Flip Flip is depicted in Figure 1.2.

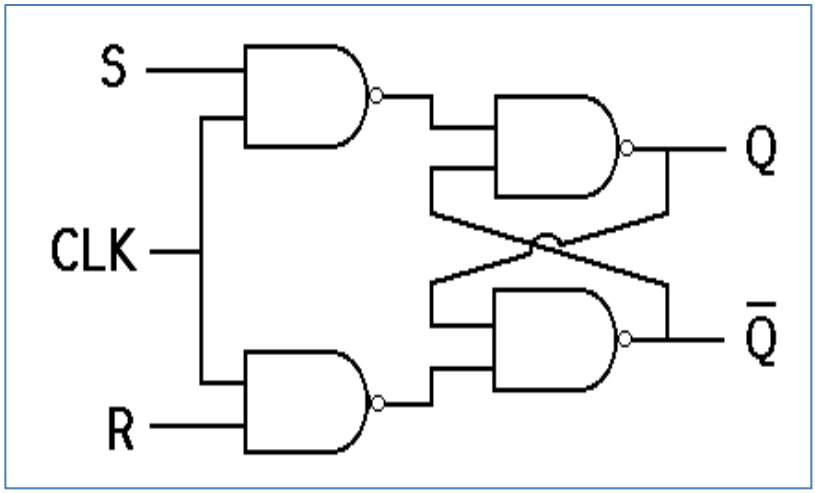


Figure 1.2 SR-FLIP FLOP

In other case, if the S value or R value is active then the output will not be changed. For better understanding of flip flops (FF), various types of FFs are discussed here which are applied for different applications.

1.3.2 Various Types of Flip Flops

There are four kinds of Flip Flops such as SR, JK, D and T type Flip Flops which are available in the circuit design industry.

1.4 SR FLIP FLOP

One of most common Flip Flops is the SR Flip Flop. This SR-FF is very easy to understand and it is simple as shown in Figure 1.2. It produces two outputs; they are inverse to each other. Based on the inputs, the outputs generated by a SR Flip Flop are given in Table 1.1.

Table 1.1 SR Flip Flop Input Vs. Output

S.NO	S	R	Q	Q’
1	0	0	0	1
2	0	1	0	1
3	1	0	1	0
4	1	1	∞	∞

1.5 JK FLIP-FLOP

It is necessary to go for other Flip Flop in the electronic circuit industry because of the undefined state obtained in SR Flip Flop. Hence, JK Flip Flop is considered as an improved version of SR – FF, since S=R=1 is not considered as a problem. The logic diagram of JK-Flip flip is depicted in Figure 1.3.

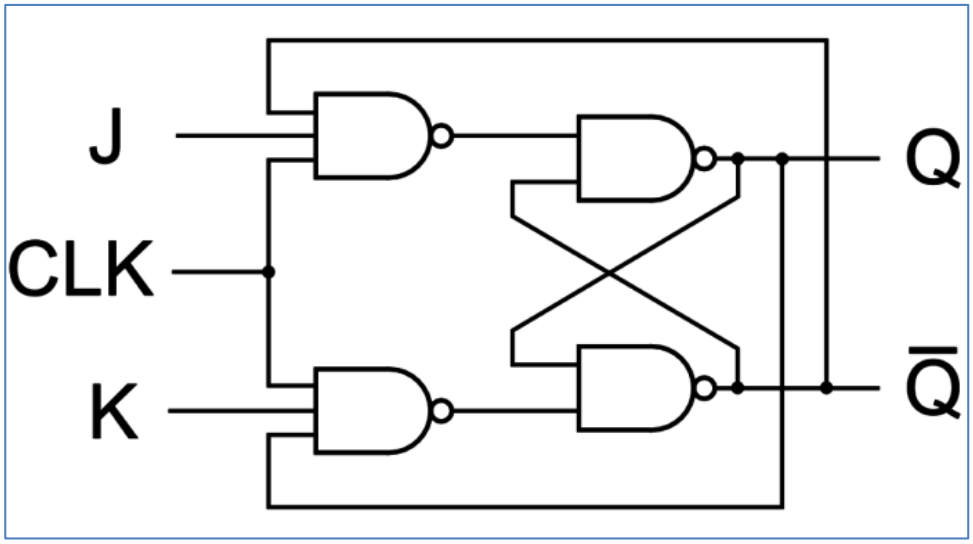


Figure 1.3 JK-FLIP FLOP

In this JK Flip Flop, when J=K=1 condition occurs, the JK-FF generates an output which inverts the state of the output. The results based on the input of JK-FF is given in Table 1.2.

Table 1.2 JK Flip Flop Input Vs. Output

S.No	J	K	Q	Q'
1	0	0	0	0
2	0	1	0	0
3	1	0	0	1
4	1	1	0	1
5	0	0	1	1
6	0	1	1	0
7	1	0	1	1
8	1	1	1	0

1.6 D FLIP FLOP

One of the alternatives for JK Flip Flop which is better than JK is D Flip Flop. D FF is popular in digital electronics and they are used in shift registers, counters and synchronizing the input. The logic diagram of D-Flip Flip is depicted in Figure 1.4.

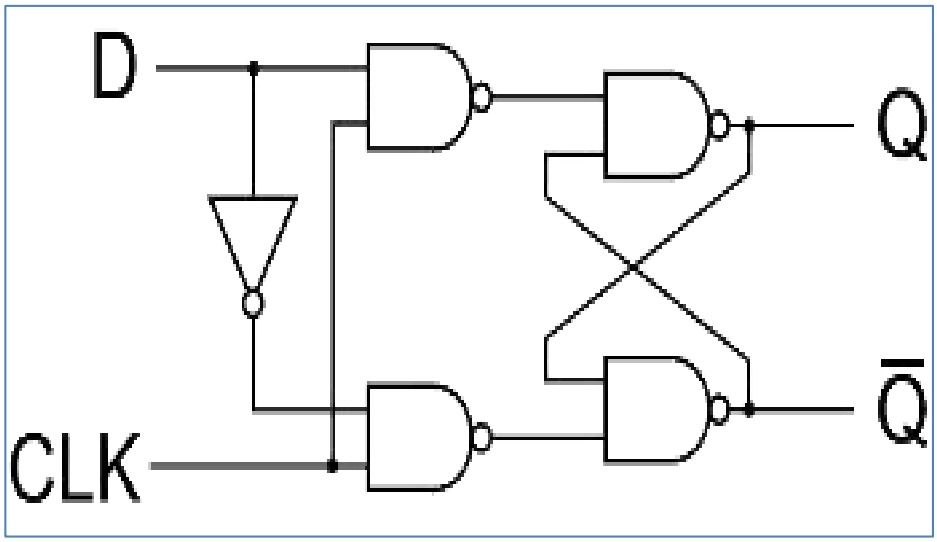


Figure 1.4 D-FLIP FLOP

The output of the D Flip Flop gets changes only at the clock edge. Other than that, even if the input changes, it does not affect the output. It is shown in Table 1.3.

Table 1.3 D Flip Flop Input Vs. Output

S.NO	CLOCK	D	Q	Q’
1	↓>>	0	0	1
2	↑>>	0	0	1
3	↓>>	1	0	1
4	↑>>	1	1	0

The change of state of the output is depends on the rising edge of the clock. The output (Q) is same as the input and can only change at the rising edge of the clock.

1.7 T FLIP FLOP

The T Flip Flop is like JK Flip-Flop. These are basically a single input version of JK Flip Flop. This modified form of JK Flip Flop is obtained by connecting both inputs J and K together. This Flip Flop has only one input along with the clock input. It is shown in Figure 1.5.

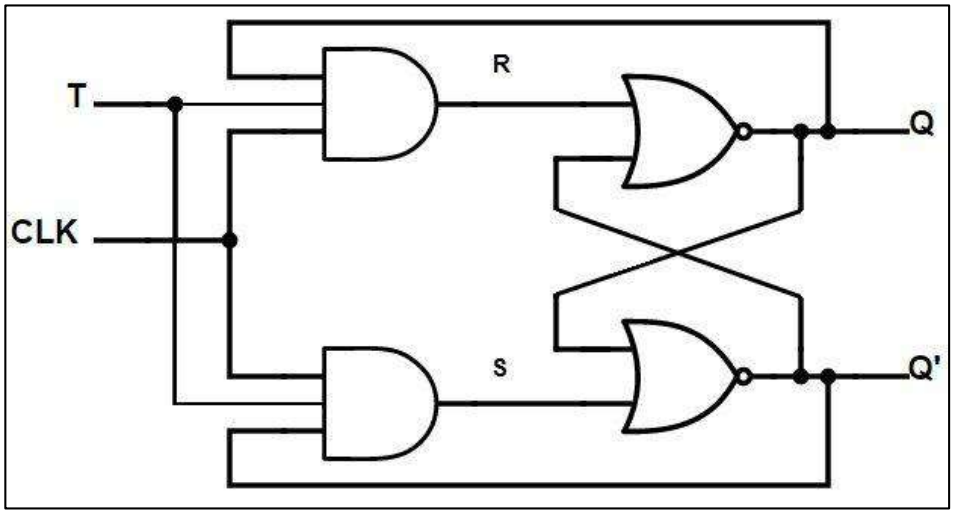


Figure 1.5 T-FLIP FLOP

These Flip Flops are called T Flip Flops because of their ability to complement its state (i.e.) Toggle, hence the name Toggle Flip-Flop. The output is shown in Table 1.4 based on input.

Table 1.4 T Flip Flop Input Vs. Output

S.NO	CLOCK	T	Q	Q(t+1)
1	0	0	0	0
2	1	0	1	1
3	0	1	1	1
4	1	1	1	0

1.7.1 Applications of Flip-Flops

A group of Flip Flops connected together forms a register. A register is used solely for storing and shifting data which is in the form of 1's and/or 0's, entered from an external source. It has no specific sequence of states except in certain very specialized applications. A counter is a register capable of counting the number of clock pulses arriving at its clock input. Count represents the number of clock pulses arrived. A specified sequence of states is different for different type of counters.

There are two types of counters, synchronous and asynchronous. In synchronous counter, the common clock input is connected to all of the Flip Flops and they are clocked simultaneously. In asynchronous counter, commonly called, ripple counters, the first Flip Flop is clocked by the external clock pulse and then each successive Flip Flop is clocked by the Q and Q' output of the previous Flip Flop. Therefore in an asynchronous counter, the Flip Flops are not clocked simultaneously.

These are the various types of Flip Flops being used in digital electronic circuits and the applications of Flip Flops are as follows -

- Counters
- Frequency Dividers

- Shift Register
- Data Transfer
- Storage Register
- RAM
- Oscillators
- Switch Debouncing

Flip Flops are almost used in every field of Digital Electronics today, since they are the most vital part of a sequential logic circuit. Most of the applications of a sequential circuit use the clock operations of the Flip Flop. Some the applications of the flip-flops are explained in detail below.

1.7.1.1 Counters

A counter is basically a sequential circuit. They are designed by using Flip Flops. Counters are the most used application of the Flip Flops. They are constructed with a group of Flip Flops along with a clock signal. In digital electronics, counter is a device that can store and displays and count the output of the total number of time an event or state has occurred in a circuit at predefined time. In a counter the number of states that has occurred is known as the “MOD NUMBER”. It is able to count both up and down based on the input pulse given and can also follow any sequence of event that is generated according to the circuit design.

The counters can be classified into two different types based on the arrangement of the Flip Flops.

1.7.1.2 Asynchronous Counter

An asynchronous counter is also known as a RIPPLE Counter. This counter can be constructed from a Toggle or a JK Flip Flop. A main clock pulse is given to the first Flip Flop and the rest of the clock circuit gets the signal from the output (Q) of the previous Flip Flops. For every clock signal, the output changes. Thus, an asynchronous counter does not have a universal clock. The Figure 1.6 shows a four-bit design counter.

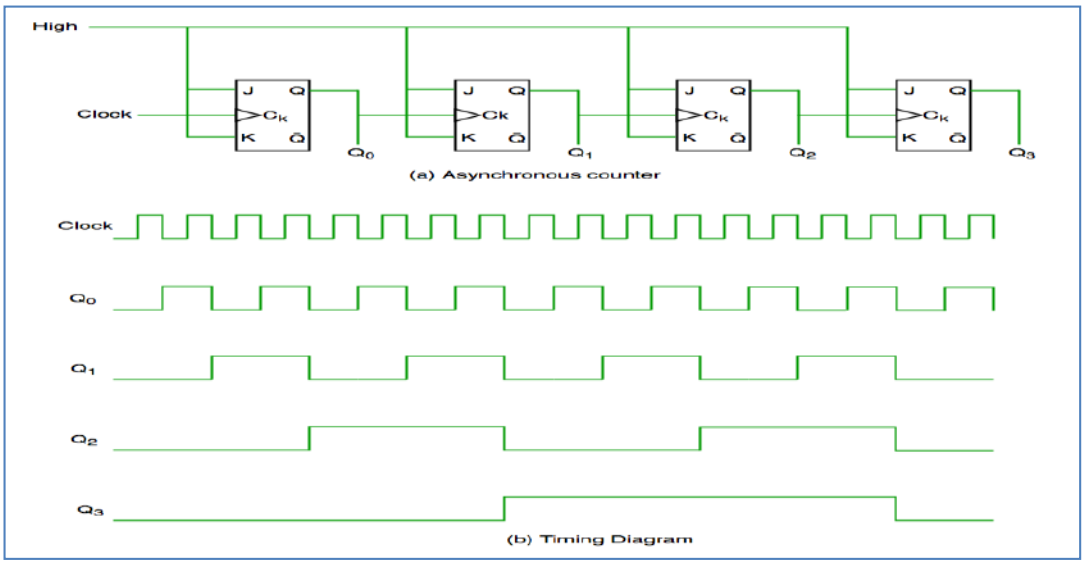


Figure 1.6 Asynchronous counter

The Figure 1.6 shows the timing diagram of the asynchronous counter. Let us consider a counter designed with four Flip Flops, then the outputs will be Q_0, Q_1, Q_2 and Q_3.

The clock input is given to first Flip Flop. As soon as the clock is triggered, the output Q_0 changes, when the clock pulse starts to go low from High i.e. when the rising edge of the clock pulse is encountered, likewise, the output of Q_1 changes state when the output of Q_0 starts to go low. Here, the output of the previous Flip Flop is the clock signal of the next Flip Flop.

This process continuous for the rest of the Flip Flops causing asynchronous pattern of the ripple generation all through the outputs, hence the name ripple counter.

1.7.1.3 Synchronous Counter

The synchronous counter has universal clock as shown in Figure 1.7. Here, each Flip Flop is excited at the same time by one global clock. So, the output of each Flip Flop changes simultaneously.

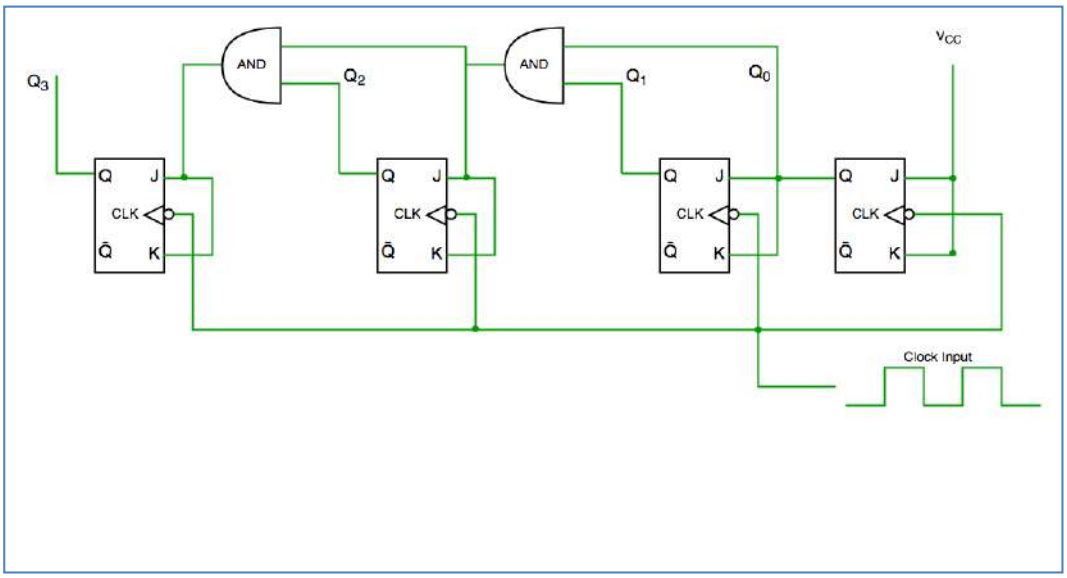


Figure 1.7 Synchronous Counter

A synchronous counter is able to operate during high frequencies. Since, the same circuit input is given to each Flip Flops in a synchronous counter; there is no any cumulative delay in it.

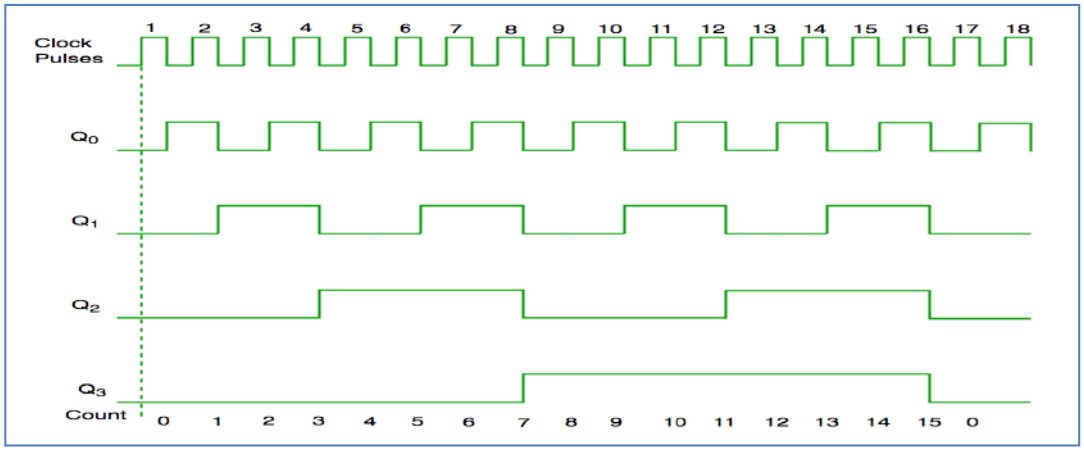


Figure 1.8 Timing Diagram of a Synchronous Counter

In an asynchronous counter, each Flip Flop will be driven by the signal from the previous Flip Flop, so the output of each Flip Flop depends on the output of the previous Flip Flop. Here, the output depends on all the previous Flip Flops output. The output Flip Flops responses to every falling edge of the clock pulse, i.e. Q_1 changes with respect to Q_0, Q_2 depends on the state of both Q_0 and Q_1. Q_3 depends on the state of Q_0, Q_1. and Q_2 as shown in Figure 1.8.

Both the synchronous counters can be classified further by their counting progresses, they are

(i) Up Counter

(ii) Down Counter

(iii) Up/ Down Counter

1.7.1.4 Decade Counter

A Counter that can count up to 10 states or events in the series is known as a Decade Counter. This counter resets itself once it reaches the state

from 0000 to 1001 i.e 10 states or events. Decade counters are widely used in digital electronics.

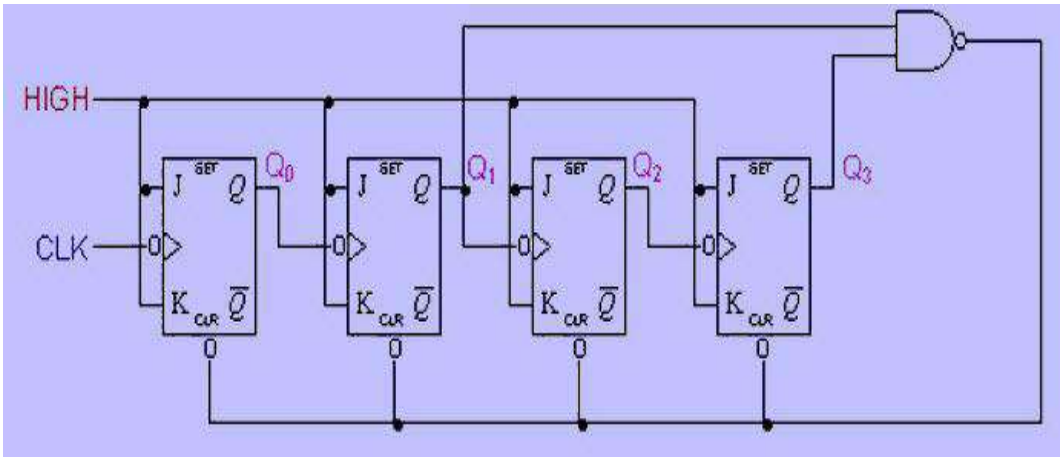


Figure 1.9 Decade Counter

They come as a part in big integrated circuits. Decade counters are available in the form of IC's. A Decade counter can come as both Asynchronous decade counter and Synchronous decade counter. The binary counter has maximum number of states equal to 2^n, where n is the number of flip-flops in the counter. Counters can also be designed to have a number of states in their sequence that is less than 2^n. In decade counters the sequence is truncated up to ten states, 0000(0 in decimal) through 1001(9 in decimal). These types of counters are very useful in display applications in which BCD numbers are used.

The truncation in the count sequence is achieved by resetting the counter at particular count instead of going through all of its normal state. In case of BCD decade counter sequence is reset back to the 0000 state after the 1001 state. The resetting of counter is done with the help of reset inputs of each flip-flop. These inputs are activated when desired state is reached. In case of BCD decade counter, reset output is activated using NAND gate when 1010

state is reached. Figure 1.9 and Figure 1.10 shows the asynchronous decade counter.

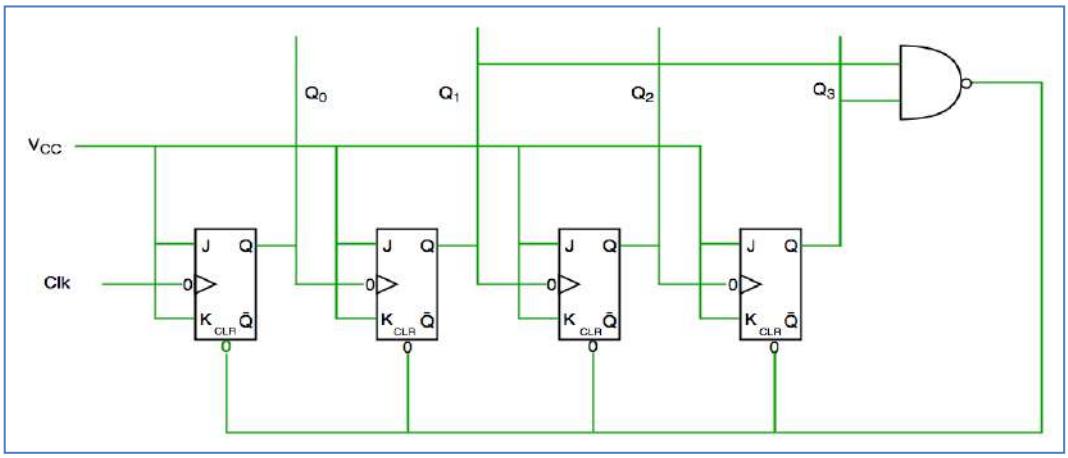


Figure 1.10 Asynchronous Decade Counter

The Truth table of Decade Counter is shown in Table 1.5.

Table 1.5 Decade Counter Input Vs. Output

S.NO	CLOCK COUNT	Q1	Q2	Q3	Q4
1	1	0	0	0	0
2	2	0	0	0	1
3	3	0	0	1	0
4	4	0	0	1	1
5	5	0	0	0	0
6	6	0	1	0	1
7	7	0	1	1	0
8	8	0	1	1	1
9	9	1	0	0	0
10	10	1	0	0	1
11	11	Counter resets its outputs back to zero			

1.7.1.5 Frequency Divider

The frequency of a periodic waveform can be divided by using a Flip Flop. If Flip Flops are used to build a circuit for this purpose it is called as a frequency divider. It can also be called as a scalar or a pre-scale or also as a clock divider. The frequency divider circuit receives an input frequency say F_i and it generates an output frequency F_o, which is only half the value of the input frequency given. This process can be explained with the following formula,

$$F_o = F_i / n$$

Where,

F_i - input frequency.

F_o - output frequency.

n - can be any integer.

These frequency dividers can be used in analog as well as in digital circuits. We can use a Delay Flip Flop or Toggle Flip Flop or JK Flip Flop in a frequency divider circuit.

1.7.1.6 Shift Register

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to a group of registers called “shift register”. They are very important in applications involving the storage and transfer of data in a digital system. A Flip Flop can store only

one bit of information in it i.e. either 1 or 0. We can use multiple numbers of Flip Flops if we need multiple storage. This multiple set of Flip Flops used in a sequential circuit to store binary data which are called as “Register”. The amount of data that is stored in a register is directly proportional to the number of Flip Flop circuit.

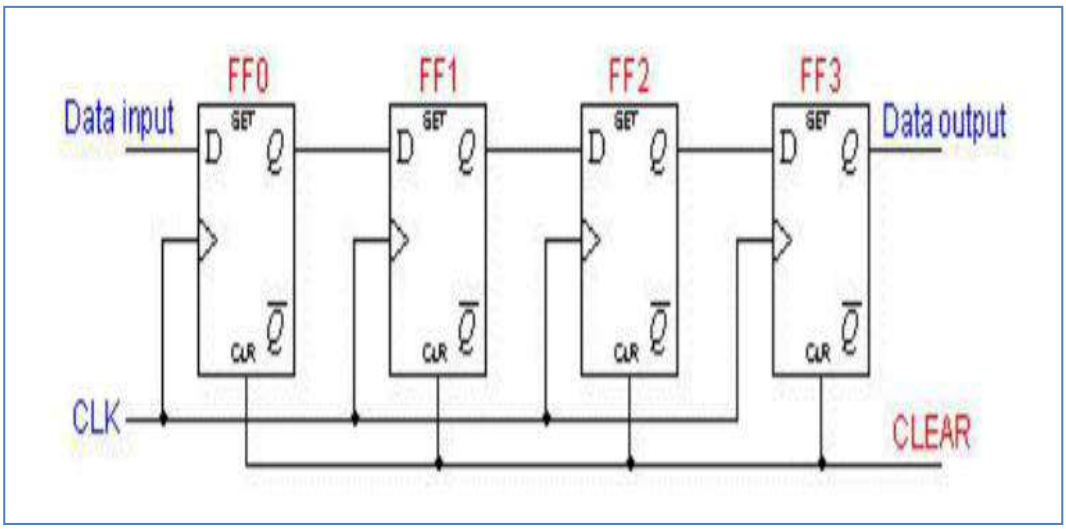


Figure 1.11 Shift Registers

These Registers can, further be called as “Shift Register” when they are able to shift the binary data in the Flip Flops from right to left (right shifting) or left to right (left shifting). If we use ‘N’ number of Flip Flops in a circuit, then it can be called as “N Bit Shift register”. A simple shift register consists of a chain of delay or data or D Flip Flops connected in series. Depending on the arrangements of this inputs and outputs in these shift registers, they are classified into four main types. The data will shift from one Flip Flop to another from each positive edge trigger of the clock pulse, as shown in Figure 1.11. The major classifications of shift registers are as follows:

1.7.1.7 Serial In – Serial Out (SISO) Register

The purpose of the register is to transfer data throughout the Flip Flops. Before any clock signal is given the register is completely cleared so that all its output is '0'.

In this Serial In – Serial Out Register the input data is applied to the D Flip Flop at the left most end and the output is received serially on the right most in the same way, one after the other. Hence the name is called as SISO Register, shown in Figure 1.12.

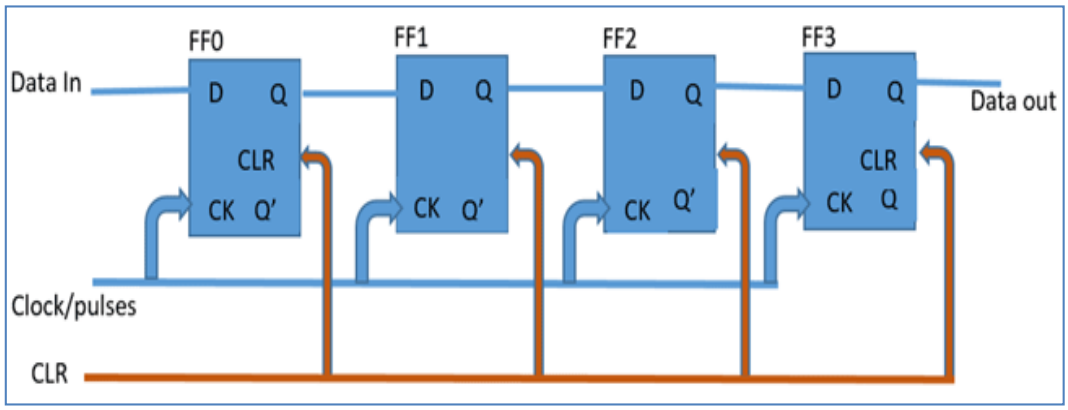


Figure 1.12 SISO Register

The Figure 1.12 shows a four bit Serial In – Serial Out Shift Register. Here, Four D Flip Flops are cascaded, which means the output of every D Flip Flops is connected to the input of the next D Flip Flop in a clock wise order. Since, the clock pulse applied to each Flip Flop is same, they are said to be synchronous with each other.

1.7.1.8 Serial In – Parallel Out (SIPO) Register

The Serial In – Parallel Out register is similar to Serial In – Serial Out register as far as the input signals are applied. In this register, we use the

same D Flip Flops. FFs are cascaded and the input signal is sent via right shifting method in to the Flip Flops. But, in Serial In – Parallel Out, the data in is applied in serial manner and the output is taken from the Flip Flop in parallel manner and it is shown in Figure 1.13.

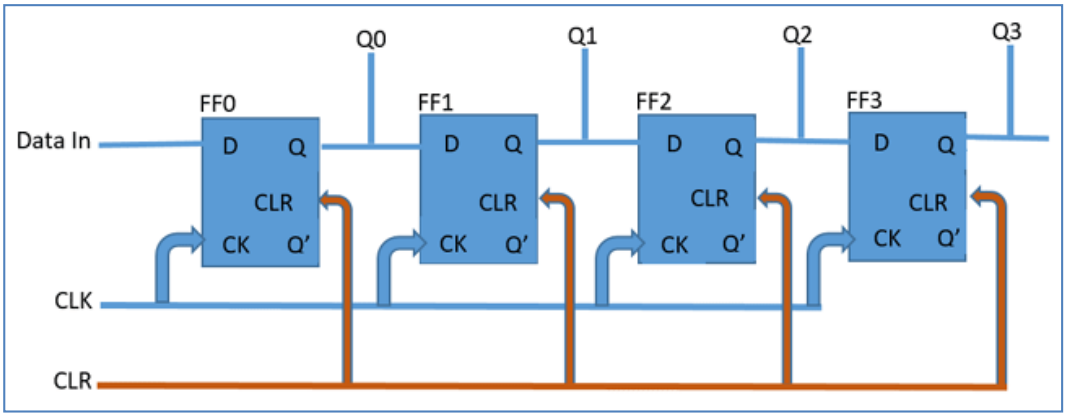


Figure 1.13 SIPO Register

The truth table for SIPO Register is shown in Table 1.6.

Table 1.6 Truth Table for SIPO Register

S.NO	CLOCK PULSE NO	Q0	Q1	Q2	Q3
1	0	0	0	0	0
2	1	1	0	0	0
3	2	0	1	0	0
4	3	0	0	1	0
5	4	0	0	0	1
6	5	0	0	0	0

1.7.1.9 Parallel In – Serial Out (PISO) Register

In case of Parallel In – Serial Out register, the data to each D Flip Flop is applied parallel and the output is taken in serial manner when the enable input is in set condition.

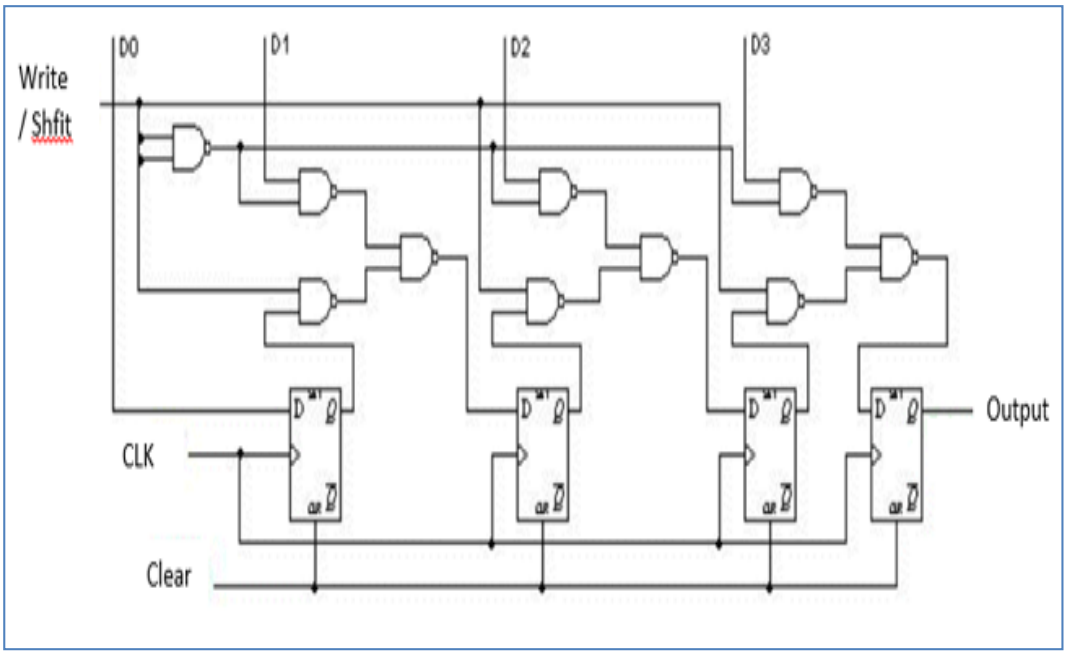


Figure 1.14 PISO Register

The data shift registers through the register for each positive edge triggering of clock pulse thus producing a serial output on the right end of the register, is shown in Figure 1.14.

1.7.1.10 Parallel In – Parallel Out (PIPO) Register

A Parallel In – Parallel Out shift register can be made into a temporary storing device or as a time delaying device. The entire Flip Flops have the same clock pulse, as it is in all the other types. The main difference in this register is that, each Flip Flop receives a separate parallel data input and hence produce parallel data output correspondingly. Hence the name Parallel

In – Parallel Out Shift Register. A shift register that is constructed with all the above described combination in a single device is called as a universal shift register, as shown in Figure 1.15.

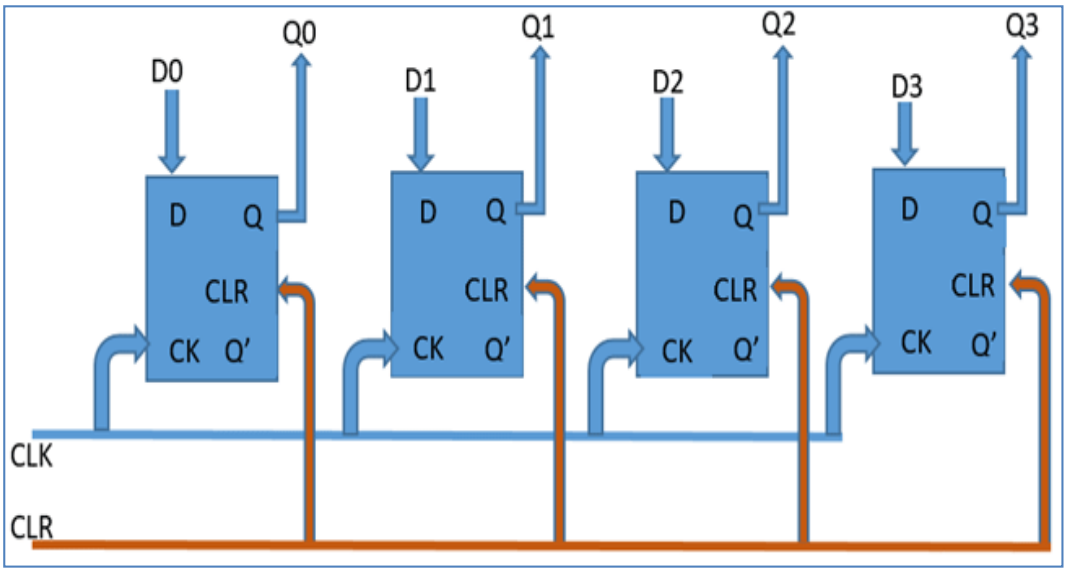


Figure 1.15 PIPO Register

1.7.2 Other Formations of Flip Flops

The latching elements have been imposed on number of clocking formats with limitations by the digital structure to conclude their usage in various systems. Frequently employed schemes were single phase and dual phase clocking. The investigation on the time involvement in synchronous digital schemes was exhibited elaborately in the work (Abu-Khater *et al.* 1996). A contrast investigation between the Flip-Flops and latch applications in highly performing systems were completed and published in research works (Chandrakasan *et al.* 2000) and (Esmaeili *et al.* 2012). This evaluation was the trade-offs between the velocity, power and time delay the system.

With the nature of low power consumption and appropriate time restrictions, timer devices, latches and Flip Flops were involved in the digital

systems. In the high-performance systems, the clock generating arrangement is primary as it consumes a major portion of the total power consumption in the total system, which was explained by (Esmaeili *et al.*2010*)*. For better performance, short network setup and hold time is more essential, that is mostly disregarded. During the experiment and analytic process, the information from the Flip Flops within and outside of the system has to be recorded in a multifaceted arrangement.

The number of logic levels between the channel phase has to be reduced as the frequency increases, so that some part of the logic has to be entrenched in the Flip Flops. In the minimum cycle times, the clock skew increases in depth in the micrometre designs, where it doesn't follow the technical scaling, meanwhile the absorption of clock skew in a stipulated time is much more significant. This supplement requisites forced on the latches has to be given equal significance with their performance characteristics. The total time taken from the device is the addition of erection time and the clock to output delay.

The time elapses between the last point of data arrival and the yield conversion measures the device delay time. Intrinsic parallelism is revealed in the cavernous channel system, which entail vast fan out in the output of the register. With superior driving strengths, the devices can be operated with minimum delay time, examples can be represented with the sense-amplifier-based flip-flop (SAFF) investigated by (Cooke *et al.* 2003), Hybrid Latch Flip-Flop (HLFF) analysed (Fuse *et al.* 2001) and semi-dynamic flip-flop (SDFF) recommended by (Hesley *et al.* 1999), (Hu. *et al.*2007).

Sense-Amplifier-based flip-flop is restricted by the latter ones, due to its limitation in erecting the output latch.

1.7.3 Flip-Flop with Sensing Amplifier

The block diagram in Figure1.6 illustrates the operation of Flip Flop which is discriminated from the master slave (MS) which has a combination of two parallel latches. If it is not assured with suitable margin between two phases of clock, the MS pair will be translucent. The unit comprises of dual parts designated pulse generator (PG) and slave Flip Flop comparable to MS unit master and slave bistable multivibrator. The functional output of the data and clock signal is the primary stage in the structure. If there is variation in the data and clock signal output, the pulses with different width can be yielded which sets slave latch. The later stage is sensitive to the clock transition (From 0 to 1 or 1 to 0) and not to the level as in MS grouping. The flexibility and quality of the function of them may be endangered sometimes due to the sensitive implementation of PG level

Due to this risk level in the employment of Flip Flops, it has been avoided in few methodologies like LSSD of IBM that is illustrated by (Kawaguchi *et al.* 1997). The sensory amplifier maintains that first stage and slave relay adheres to the second stage. The Generic internal Flip Flop framework is shown in Figure 1.16.

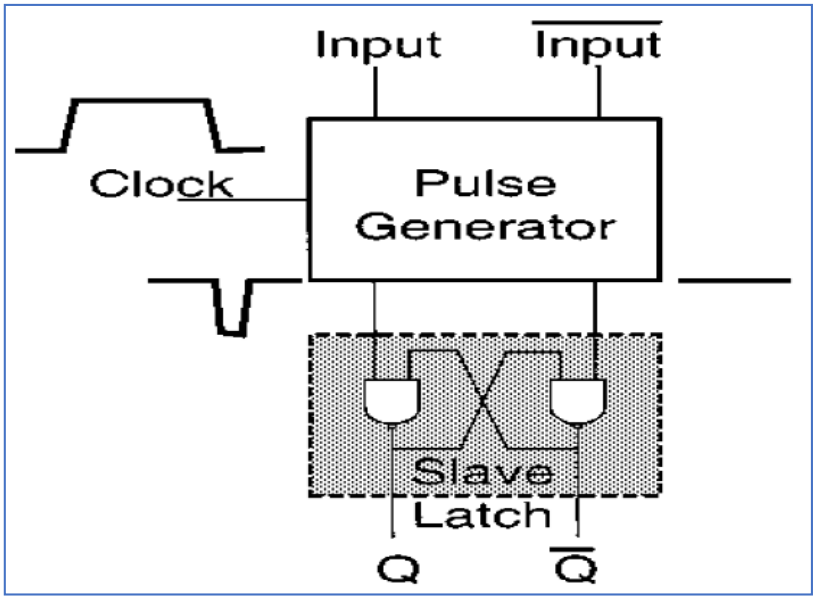


Figure 1.16 Generic internal Flip Flop framework.

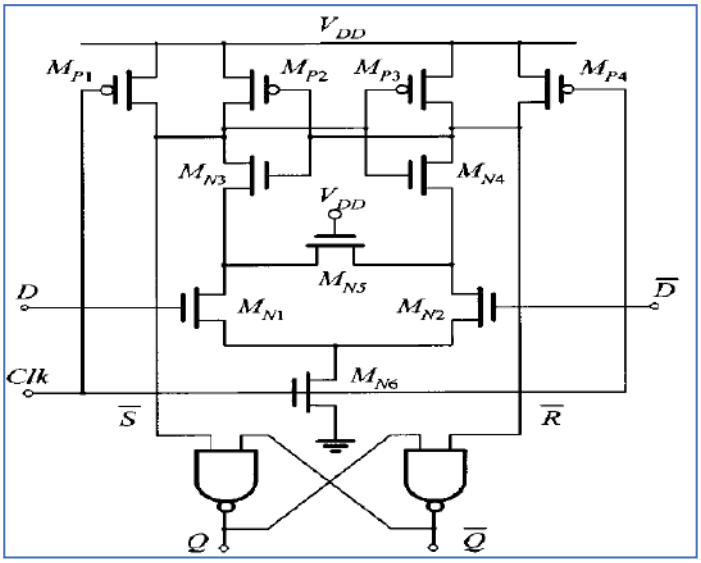


Figure 1.17 Sense Amplifier Flip Flop

According to the requirement, a negatory signal is supplied to the single terminal port as required to be configured or to restart. As illustrated by (Chiou *et al.* 2007), (Chung. *et al.* 2002), SA is a pulse producing module in this SAFF, as shown in Figure 1.17. This senses the real and discrepancies in the inputs .Tracking the leading clock edge, a monotonic variation from high to low level in any one of the outputs was generated by the

SA stage. The output of SA will not be influenced even if there is any disparity in the data clock intervals. Unless the next leading edge prevails, the SA latch holds the state and won't leave for any transition. Once the clock shifts to inactive mode, the two outputs of this module reach a high level which leaves the module to proceed as Flip Flop.

Apart from the above types of Flip Flops, the other Flip Flop circuits developed for low power and high-speed performance applications is discussed in Chapter 3 as existing design methods and the outputs of the Flip Flops are customized. Clock Gated Edge activated Sense enhanced Flip Flop is evaluated. Countdown Gated Sense Modulated Flip Flop, Edge Activated Sense Modulated Flip Flop and Dual Edge Activated Sense Modulated Flip Flop is included with current development methods.

1.8 SUMMARY

This chapter presents the logic diagram, truth table based functionalities and merits and demerits of various types of Flip Flops. From this chapter, it is understood that, based on the application and performance requirement, simple flip flops with easy internal structure can be modified and designed which can be applied for various applications. Chapter 2 provides a detailed survey about various earlier research methods and its issues and challenges.

1.9 RESEARCH PROBLEM

Flip Flop is the basic component in digital electronic circuits, which are used in various power circuit applications. Flip Flops are used for storing the data. It is necessary to reduce the power consumption and to increase the speed. For this purpose, FF circuits are incorporated with clock gates, edge

amplifiers, dual edge triggering techniques and so on. Several existing FF architectures are analysed. In terms of limitations, Modified Clock Gated Sense Amplifier (MCG-SA) based FF circuit is designed which has advantages like speed in operation, less area utilization and low power consumption. The proposed MCGDET-SAFF circuit is simulated by different methods within digital channels like DSP. The first MCG-SAFF is used to obtain a considerable power lessening by integrating DET mechanism and conditional pre-charging. Also, by exhausting speed of the symmetrical latch, the MCGDET-SAFF is capable of accomplishing lower power dissipation and delay. The proposed design has considered the baseline circuit and it is developed as a novel CGFF to decrease the power dissipation further at low switching activity and the second proposed FF design gives more power savings additionally.

1.10 RESEARCH OBJECTIVES

The main objective of this research work is to design and implement a modified clock gated dual edge-triggered sense amplifier Flip Flops for low power, less area and high-performance applications. To obtain the main objectives, some of the additional objectives are carried out. They are,

- To design a dual edge triggered sense amplifier Flip Flop with a symmetric latch for high performance and low power applications.
- To reduce the power consumption by decreasing the clock switching power, to reduce the delay and to avoid power leakage.
- To propose an improved feedback path thereby, to obtain the desired power dissipation.
- To reduce the area of the silicon by using smaller number of transistors in the clock gating method.

- To propose a sense amplifier FF that minimizes the delay and increases the pace of the systems.

1.11 RESEARCH METHODOLOGY

This research work proposed a modified clock gated dual edge triggering sense amplified Flip Flop (MCG-DET-SAFF) design for low power, high speed applications. Devices in electronic circuits are needed to be power efficient, since they are most important concern when they are integrated with large scale circuits. Flip Flops are mainly used in pipelining techniques which needs more power efficiency. Pulse triggered Flip-Flop (PT-FF), Transmission gate FF (TG-FF), Master-Slave FF are the main classes of Flip Flops. Pulse triggered Flip Flops (PTFFs) have advantages in terms of speed and low power consumption. It has two types such as implicit and explicit PTFF. Explicit PTFF (EPTFF) has latch and separate pulse generator and it is more efficient in power consumption but low in speed. To increase the speed EPTFF needs to be modified. Clock gating method eliminates unnecessary power dissipation in clock switching; therefore, it is considered as an efficient method. It is used in FFs to reduce power dissipation dynamically. Power dissipation can also be obtained by diminishing clock switching. Dual edge triggered flip with clock gating can reduce the power consumption and memory utilization. Hence this research work integrates dual edge triggering with clock gating sense amplified FF to improve the performance regarding power, area and speed. The sense amplified FF saves power by reducing the swing design. In the sense amplified FF, the delay is not depending on the load and the output provides a small clock load and symmetrical delay. Hence this research work motivates to design and implement a modified dual edge triggered sense amplified clock gated Flip Flop for improving the performance regarding power, speed and delay.

1.12 ORGANISATION OF THESIS

The entire research work is organised into a sequence of chapters as follows:

Chapter 1: This chapter presents the detailed information of Flip Flop from the fundamental to the recent VLSI circuits using Flip Flop. This chapter gives more knowledge about basic arithmetic operations and shift operations involving in VLSI circuits. It helps to understand the entire research work discussion in the other chapters.

Chapter 2: This chapter presents the various earlier research works focused on designing VLSI circuits using Flip Flops for enhancing the performance of the VLSI circuits. It helps to understand the lack and demand of Flip Flops and the research problem which needs a better solution.

Chapter 3: This chapter presents the existing methodologies of Flip Flops applied for Low Power and High-Performance Applications.

Chapter 4: This chapter discusses about the proposed methodology of this research work with performance evaluation.

Chapter 5: This chapter discusses about Experimental Results and Discussion of this research work.

Chapter 6: This chapter presents the Conclusion and Future Work of the research work.

CHAPTER 2

LITERATURE REVIEW

2.1 OBJECTIVE

This chapter presents a detailed survey about various methods focused on designing Flip Flop circuits which can be used for low power and high-speed applications. This chapter provides introduction, recent research works of Flip Flop design methods, various Flip-flop topologies, methods used for minimizing power dissipation and power leakage with summary. From this chapter it is very easy to identify the motivation and ideas of the authors involved in earlier research works, which helps to determine the research problem and create a new design method.

2.2 INTRODUCTION

The various kinds of VLSI processors have the complete processor energy usage which is centred on electronic cycle, storage network, energy degradation and Flip Flops. These types of chips are achieved high throughput with the help of using several pipeline stages and also it increases the number of Flip-Flops in the chip. The layout therefore matters greatly as it lowers the power usage of clock stacks and Flip Flops on both ends. The big logic systems are placed in tiny fields. However, the increased relevance of power in the current years has provided the region and the velocity comparable significance. The clock system is among the most major portions of the matched VLSI module, as it can considerably impact the drop of velocity, range and energy. In particular there are four kinds of energy failures on the

CMOS grid. It changes (or dynamic) power, strength of a power surge, power of breakage and steady power.

The chip's physical part is designed with the hierarchy of transistors, macros, units and microprocessor cores which are custom and employed, SRAM and packaged. The macros, systems, base and chips have moment, region, structure, wrapping and I / O agreements when the development stage is being worked out. Timing and physical design of the chip are simultaneously made at all levels of sequence. During the design of the chip, all major buses are routed initially.

When designing the VLSI (Very Large-Scale Integration) systems, energy usage is a key consideration in small energy applications in specific. In view of the growing request for small-scale energy applications, micro-power thermal loops and Flip Flops need to be designed (Liu *et al.* 2006, Kim *et al.* 2005). The Clock Distribution Network (CDN) and latches used in this model have the most power usage parts. Those parts consume 30 to 60 percent of all energy Flip Flops (Kawaguchi and Sakurai, 1997) which produce 90 percent energy. Every day, the electricity usage of the micro processor is increasing annually only by around 20 times (Nedovic *et al.* 2002). The clocking scheme absorbs more energy because of the scaling of the load and the profound piping, thus reducing the energy usage in battery supply systems and in Flip Flops. The bandwidth utilization of the Flip Flops must also be decreased by the difficult time in high-frequency deployment (Cooke *et al.* 2003, Hofstee *et al.* 2000).

Multi-plan synchronization on 3-D VLSI systems creates greater energy usage at elevated concentrations (Pavlidis *et al.* 2010). The storage voltage has a polynomial impact because of vibrant energy and also results in a reduction in energy (Kim *et al.* 2005). When the load voltage lowers, the

device security declines instantly. When the boundary voltage of the transistor falls, the voltage spillage is increasing (Kim *et al.* 2005, Roy *et al.* 2003). The power usage methods required without influencing the demand with decreased latency. Therefore, one technique of Clock Distribution Network (CDN) in energy reduction is dual-edge activation. The CDN frequencies are reduced by reducing the capacity to 50 times without influencing the flow rates (Nedovic and Oklobdzija 2005, Nedovic *et al.* 2001, Esmaeili *et al.* 2009, Chiou and Lou 2007, Esmaeili *et al.* 2010) by using Dual-Edge Triggered Flip-Flops (DETFFs). Single Edge-Triggered Flip-Flops (SETFFs) (Nedovic *et al.* 2002) use flip-flops to sample information on both increasing and dropping surfaces and reverse the clock rate. Dual-Edge Triggered Sense Amplifier Flip-Flop (DET-SAFF) uses a scheme that is extendable to allow double-edge triggers in any vibrant CMOS logical system outlined in it. However, this technique alters the vibrant single-edge model and increases the region. Until now, all double-edge scheduling systems have been implemented to change the one-edge activated Flip-Flop loop (Ghadiri and Mahmoodi 2005, Hu and Zhou 2007, Stojanovic and Oklobdzija 1999, Kim and Kang 2002).

This technique can be used to allow a double edge to be triggered by the variables of power usage and reduced region within any vibrant CMOS logic loop. Simultaneously, without the need to change the composition of the single-edge vibrant logic grid. In view of the difficulties encountered in the current Flip-Flop design, this work implemented a fresh suggested technique used by Sense Amplifier-Based Flip-Flop Circuits (SAFF) because of its variable features, velocity of procedure and low power usage. High performing Flip Flops (Cooke *et al.* 2003; Nedovic *et al.* 2002; Ghadiri and Mahmoodi 2001; Hu and Zhou 2007) were evaluated as sensory amplification. The idea of vibrant CMOS circuit is comparable. It has pre-loading and assessment stages to investigate the effectiveness of an enhanced system of dual triggers. It has been introduced in several digital communication techniques such as

microprocessors and data handling systems. The Flip Flop can be used to measure information upon both up and down edges of the circuit. A unique Dual Edge Triggered Sense Amplifiers Flip Flop is suggested in this study.

2.3 RELATED WORKS

(Chen *et al.* 1999) discussed reducing leakage power through integrated circuit stacking. A methodology submitted in this study job to pick and allocate ideal high-threshold voltage to obtain the highest yield sharing under goal efficiency limitations. The author describes a significant decline in DIBL impact due to levelling sub threshold present that creates additional leakage (Chen *et al.* 1998). A modern pivot to reduce energy dispersion on both creator and servant latches if there are no other information movements (Strollo and De Caro 2000) is available. Clock gates are used to decrease power usage and to prevent excessive loop node changing. This study outlined the tiny panel system used to regulate the D-FF clock that controls D-FF signalling when entry and result are the same. A new timing characterisation for dual-edge Flip Flops was provided (Nedovic *et al.* 2001). For any continuous circuit, the clock cycle is essential. Also, the time configuration and retaining the interface data is determined. In this field study, the clock time shall be greater than the instrument's transmission lag; more information about both the clock rate and timestamp constrain is addressed. (Nedovic *et al.* 2002) suggested a new reverse Flip Flop with dual rim triggering that will save energy by preventing node changes. Particularly in comparison to already released double-edge-driven stockings, the suggested Flip Flop is 12 times quicker and the energy-delay item is 10 percent smaller for 50 percent information operation. (Nedovic *et al.* 2002) suggested the peak voltage holding system in which the peak voltage would rely on the amount of work optimally be regulated by software. The voltage flow, linked to the core of the

MOS instrument was driven by a software command sensor, which produced a small Voltage for separate procedure (Tsividis *et al.* 1987).

If information transformations are not available, Clock gating is used to decrease electricity usage and also to protect against excessive node shifting. In this study, it is outlined as the tiny circuit system that supports D-FF clock that controls the D-FF activation once the D-FF entry and the D-FF production are the same. A new timing description for double-edge activated Flip Flops was provided (Nedovic *et al.* 2001). For any sequence system, the clock cycle is very important. Also, the time of configuration and the inputs will be decided. The clock duration must be greater than the transmitting time of the instrument; more criteria are addressed in this study job regarding the clock duration and information threshold. (Nedovic *et al.* 2002) suggested a new double-edge reverse-Flip Flop which will save energy by preventing node changes. Relative to the earlier released two-edge processing components, the suggested Flip Flop is up to 12% quicker with a 10% reduced energy-lag item for 50% information operation. (Nedovic *et al.* 2002) suggested a TH-hopping system for optimally regulated limit voltage via technology based on volume of work. An application power sensor motivated the frequency supply linked to the MOS unit body resulting in low Voltage or heavy Voltage for various operations (Tsividis *et al.* 1987).

(Chung *et al.* 2003) investigated the use and execution of a double edge Triggering Flip Flop (DETFF) on poor-power, high voltage in VLSI systems. The primary benefit of using DETFF is that it enables steady performance to be maintained when working at just half a rate. For its layout, efficiency, dispersion, poor voltage and high energy application, that seems to be the DETFF, the writer likened the earlier reported studies into continuous dual-edge triggered flip-flops (DETFFs) that appears ideal for digital implementation when contrasted with each other. The two-edge memory

component (DETSE) design, describing categorization, comprehensive timing, assessment, etc, has been designed (Nedovic and Oklobdzija 2005). It defined the clocking influence on the DETSE clock distribution channel at a half-clock rate and load influence. In comparisons with largest single-edge launched memory components (SETSE), the work will present a workshop on double-edge activated Flip Flops with CPU charge, pause and inner energy usage. The small-power Dual-Edge Triggered Static Pulsed Flip-Flop (DSPFF) buildings were described (Ghadiri *et al.* 2005). They made up a double-edge signal generator and a current reverse Flip Flop with identical turning times. DSPFF's stationary characteristic prevents unwanted moves of the internal node to lower energy usage. The easy design of a double-edged wave amplifier suggested that the frequency allocation networks have small energy dissipation. The two unique double-edge-triggered Flip-Flops (Liu *et al.* 2006) are recommended. One flicker mitigates unnecessary internal node transformations when present information is identical to the prior one. Comparing with other dual band-driven twists in all feasible information processing activities, it has the lowest power gap product and its delay is lowest as well. Another suggested inner clocked integrated circuits for reverse Flip-Flop handicapped (Chung *et al.* 2001).

The double-edge activated and double-Edge Triggered Flip Flop is suggested (Chiou and Lou 2007). In the case of a multi-Voltage or multi-Voltage system, the Level Converting Flip-Flop (LCFF) uses energy conservation functions. In the shift, the author defined a new power-aware lock framework to remove inner energy. It indicates the power-conscious lock moved to small-leakage mode when run in bed mode, and still maintained its information. The particular True Single Phase Clock (TSPC) Flip-Flop has been suggested by (Pedram *et al.* 1998) with a lower limit voltage pulse Transistor and several enhanced High efficiency Application (HEA) systems. They outlined an estimate of the small clock interval and dual border energy usage of the CDN.

The suggested double-edge triggered differential conditional capturing energy recovery (DE-DCCER) flip-flop enables clock rate decreased by a ratio of 2 (Esmaeili *et al.* 2009) DCCER. They outlined the methods of modulated clocking to reduce energy considerably in comparison with squared spin clocking (Esmaeili *et al.* 2012).

2.4 RECENT RESEARCH WORKS OF FLIP FLOP DESIGNING

To understand the issues and problems, challenges and solutions, outcomes and impacts, a detailed literature review is given. This section provides a brief survey about various approaches focused on designing digital circuits for reducing the power dissipation, delay and area. In research work of (Kowsalya and Palaniswami 2014) proposed a D type FF integrated with the clock gated, dual edge and half static CLK to reduce the power consumption. The circuit comprises of two Master-latches and one half-static Slave-latch for storing data only in alternate clock pulses which is similar to the common flip flop circuits. In the research work of (Jin-Fa Lin 2014) stated and proved that modified P-FF are high speed, low power consumption than conventional Flip Flops due to the pulse separation and latch in the circuits. The power consumption is highly reduced and circuit complexity is also reduced when the P-FFs share the pulse generation. The modified P-FF using feed through structure reduces the delay as well as power dissipation.

In the research work of (Vidhya *et al.* 2015) proposed a clock gated dual edge triggered Flip Flops that are investigated with sample data of asynchronous. It produces error in output but efficient in power consumption. (Kishori *et al.* 2015) proposed a modular approach for optimizing the power consumption. It is well known that low power designs are not used in small size applications. It can also be used in high performance computational devices. The proposed design of DETFF incorporated with optimization

methods to reduce the power consumption and delay. In addition to that, an explicit pulse generator including latch and a static output exact discharge FF.

It eliminates the unnecessary transistors and redundant transition of nodes internally. (Sudeer and Ajith 2015) proposed an Embedded Logic Flip Flop (ELFF) for high performance, reduced area, power consumption and delay. The design has been obtained by merging logic function with the conventional Flip Flops. From the simulation it is proved that ELFF obtained 20% better power consumption than conventional Flip Flops. From the experiment, it is proved that the proposed ELFF can be used in 80nm CMOS technology.

The work (Paanshul *et al.* 2016), proposed an analysed report about various methods based on FF implementation to investigate the performance. FF with low power clocking system is considered as the basic circuit design. From the analysed report, it is found that Conditional Data Mapping Flip-Flop (CDMFF) obtained least power consumption. CDFF obtained high amount of power consumption than CDMFF. DET-FF obtained more consumption than CDFF, CPSFF obtained high amount of power consumption than all other FFs. The CPSFF uses multi threshold voltage CMOS method for reducing the power consumption up to 70% than the other FF designs. An implicit PTFF incorporating with dual edge technique and clock gating design is proposed by (Liang *et al.* 2016). The proposed circuit design comprises of clock gating and transmission-gate logic during the pulse generation. It disables the inverters based on conditions while input is static. It eliminates the transition redundancy with latches and internal nodes, where it reduces the power consumption.

The paper (Panahifar and Hassanzadeh 2017) discussed about low power applications using a modified signal feed-through pulsed Flip Flop. This Flip Flop comprises of a pass transistor which feeds the input directly to

output. In order to reduce the delay, the feed through transistor is modified. The paper presented by (Sheik *et al.* 2018) proposed a Modified Dual Edge Triggered Sense Amplifier Flip-Flop (MDETSAFF) suitable for low power high speed applications. A symmetrical latch is included in the proposed design. By incorporating more techniques, the proposed MDETSAFF can provide more efficiency in terms of low power consumption, delay and area. The research work done (Ahmad Karimi *et al.* 2018) stated that main impacts of D-FF design are reducing the area usage and power consumption.

So that, a PTDFF is anticipated by the author and it can be used in 90nm CMOS technology. The proposed circuit utilizes transmission-gate where it controls the input reducing the power leakage. The delay of the CLK pulse generation is reduced by changing the number of transistors. Hence the proposed modified D-FF design reduces the power consumption and delay.

2.5 A REVIEW ON FLIP-FLOP TOPOLOGIES

For the past few years, several Flip Flop topologies have been proposed. For comparative analysis, the work chooses some of the commonly used and specified topologies which are included in our benchmark and four master-slave switch Flip-Flops are included there. Transmission Gate Master Slave (TGMS) and altered inverter pulsed (mC2MOS) topology is shown in Figure 2.1 and Figure 2.4. By adding C²MOS feedback into dynamic master-slave C²MOS Flip-Flop and get the result of a pseudo-static C²MOS Flip-Flop (Weste and Eshraghian 1985), Suzuki *et al.* 1973). In Figure 2.5, it describes the difference of TGMS is derived from Power PC 603 Master-Slave Flip Flop. (Gerosa *et al.* 1994). Power PC 603 is based on the C²MOS inverters which interrupt the storage components. The fourth Master Slave Flip Flop is made of a conventional SR-latch, which is intertwined with NAND / NOR doors (Chandrakashan *et al.* 1992).

The Figure 2.6 and Figure 2.7 are shown by the next two Flip Flops called pulse-triggered latches which are based on the single latch Flip Flops. Both of these reverse Flip Flops are extremely transparent on the top of a timepiece (within a pulse). The hybrid latch Flip Flop (HLFF) layer element (Partovi *et al.* 1996) and the semi-dynamic Flip Flop (SDFF) (Klass 1998) are described in Figure 2.6 and Figure 2.7. Above two Flip Flops are included with pulse generators.

In our benchmark also have two complete dynamic Flip Flops such as the TSPC Flip Flop (Yuan and Svensson 1989) and the dynamic Transmission Gate Flip Flop (Weste and Eshraghian 1985; Rabaey *et al.* 2003). These are displayed in Figure 2.3 and Figure 2.4.

All such fast switch Flip Flops (with endpoints circulating) are more susceptible to distortion and breakage. However, the work are adding a specific range to assess their performance level with other Flip Flops. The eight different Flip Flop structures are used by topology comparison and which is used in combinations of implementation and generic cell community centres.

2.5.1 Latch-based transmission gate master-slave reverse flip-flop (TGMS)

The Switch Flip-Flop from TGMS is identified by two clock gate-based transmitting latches (Weste *et al.* 1994, Rabaey *et al.* 2003, Uyemura 1992). There are several types of transmission gateways available. For example, information or PMOS transistors are to be removed in the gate-based communication.

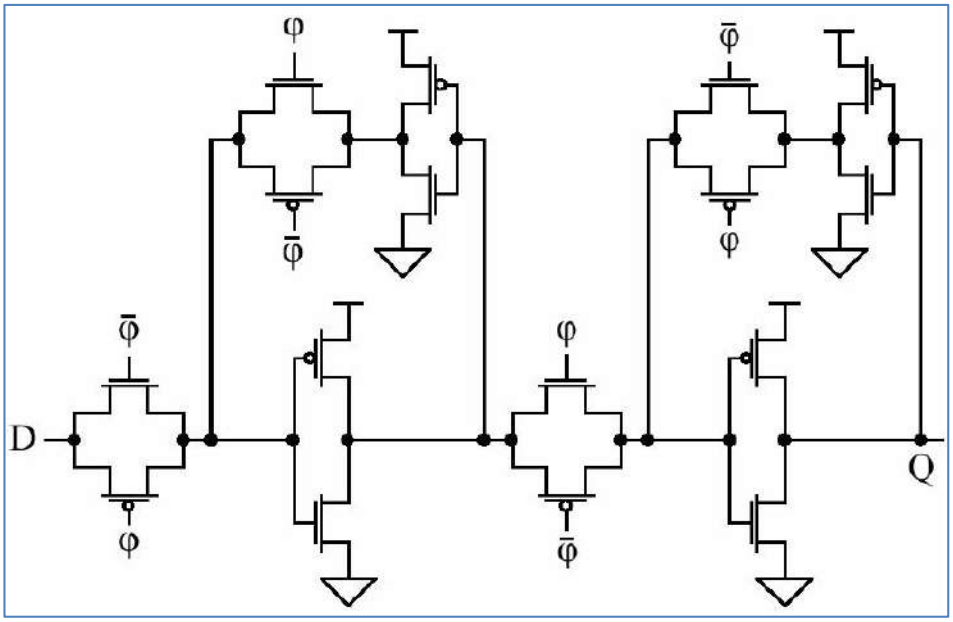


Figure 2.1 Transmitting Gate Master Slave (TGMS)

In our models, we only take into account the overall transmission portal latch presented in Figure 2.3. Later, the work compares the dynamic version of a Flip Flop into the TSPC configuration which is shown in Figure 2.6. This system uses high-speed and low power, which is sensitive to clocks. This fold-failure if clocks are overlapping the length of time. While this structure takes a high speed and low power and it is very sensitive to the overlap of the clocks. If clocks are overlapping with the length of time then the Flip Flop is failed.

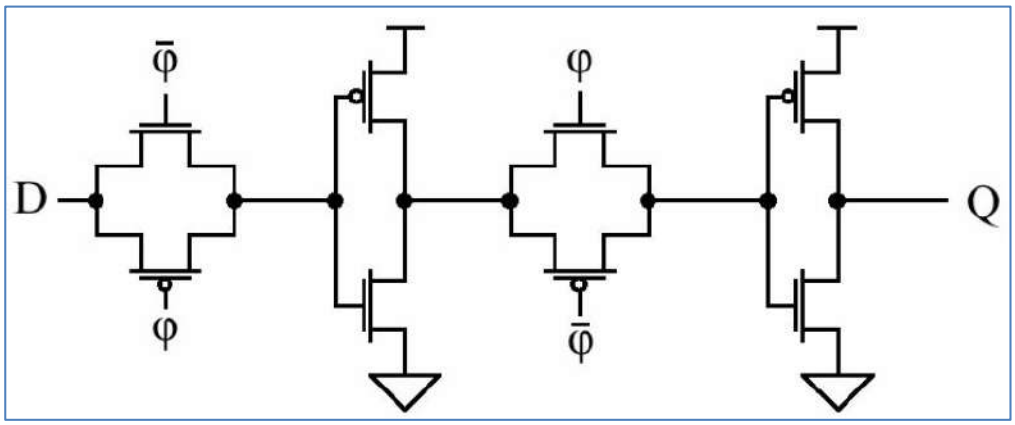


Figure 2.2 Dynamic transmission-gate flip-flop (TGMS-dyn)

2.5.2 Modified C²MOS master-slave flip-flop (mC²MOS)

The latch at Figure 2.3 can be constructed without the functional loss by removing the inverter and transmission gate for the transmission-gate based latches is used to remove a metal link, resulting in a small latch (Weste *et al.* 1994, Suzuki *et al.* 1973). Then the system is called the C²MOS latch because the clocked inverter is used by this structure. In Figure 2.4 shows the mC²MOS latch which is built by using the Flip Flop. In contrast to the Flip-Flop transmission gate, this system cannot intersect the clock.

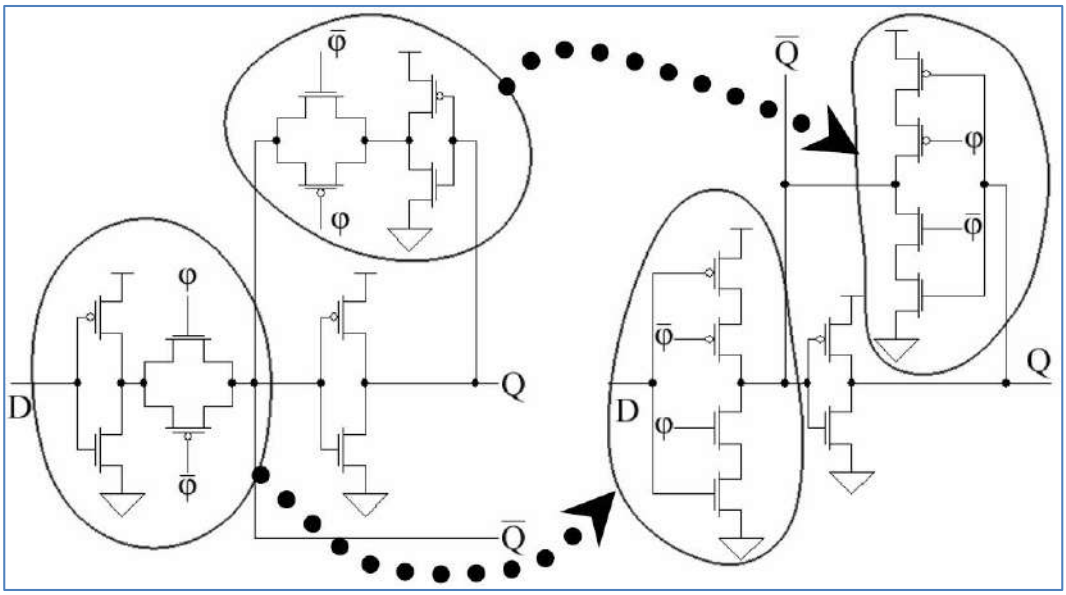


Figure 2.3 Transmission gate latch and C²MOS latch

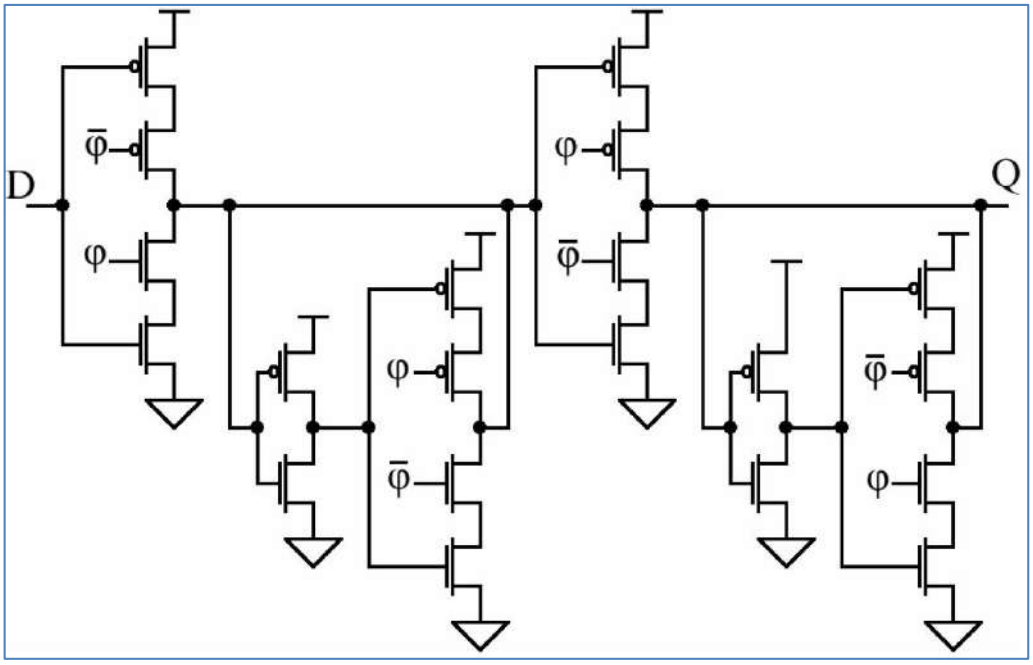


Figure 2.4 mC²MOS flip-flop

2.5.3 PowerPC 603

PowerPC 603 is the mixture of TGMS Flip Flops and mC2MOS Flip Flops. A clocked alternator will substitute the response transmission gate, as shown in Figure 2.5 (Weste *et al.* 1994, Gerosa *et al.* 1994).

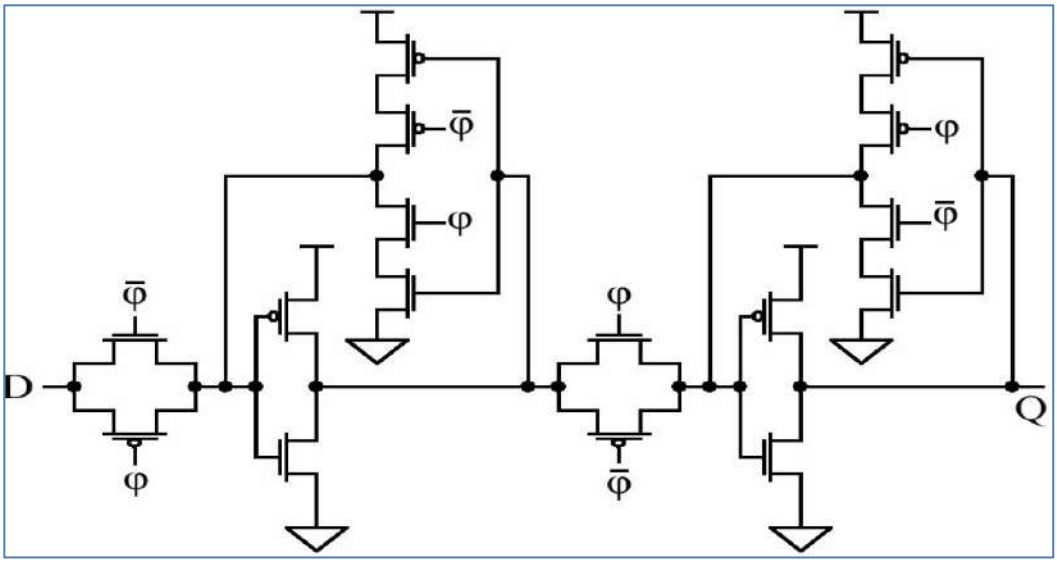


Figure 2.5 Power PC 603 flip-flop

2.5.4 9T TSPC flip-flop (TSPC)

The development of NORA-CMOS technique which introduces the True Single-Phase Clock (TSPC) CMOS circuit technique (Yuan and Svensson 1989). These methods are used to solve the issue of transmitting multiple signal transmissions and to prevent the major clock skew issues. Increased advantages include the allocation of a single board, tiny space for dial rows, elevated velocity and no clock skew.

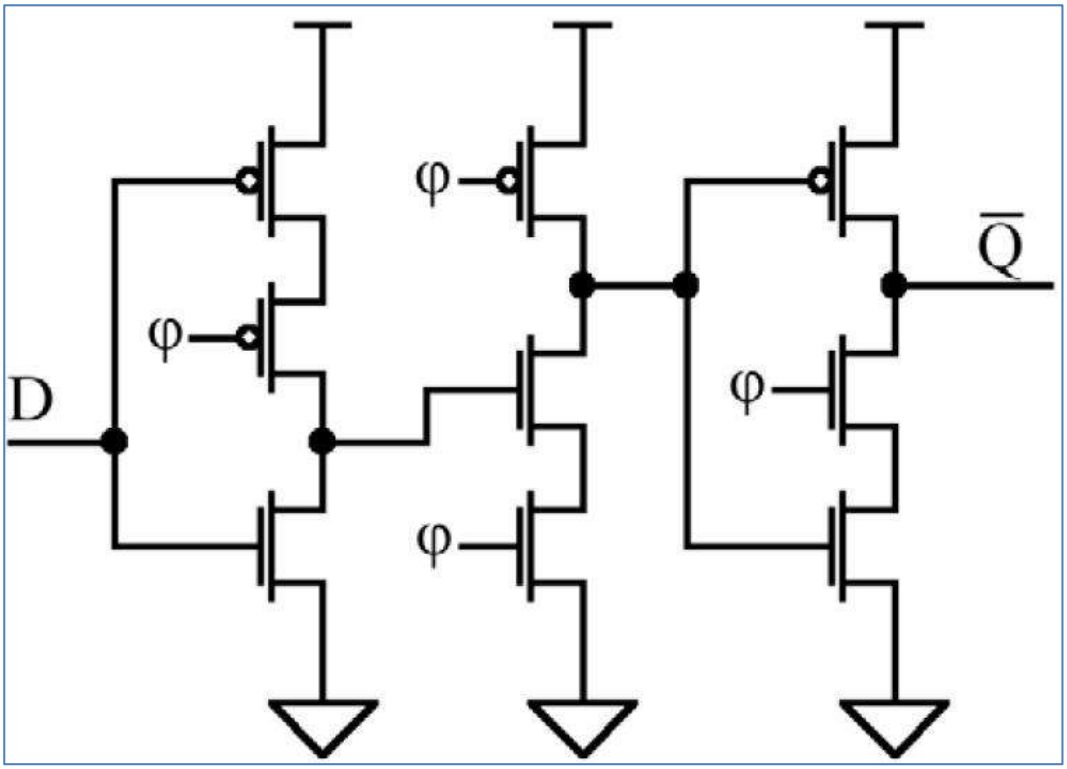


Figure 2.6 9T True single-phase clock flip-flop (TSPC)

The TSPC latches are found in different ways with the help of developing all basic essential components. The eight-transistor positive edge-triggered D Flip Flop is developed by using split-output TSPC latches (Yuan and Svensson 1989), which is shown in Figure 2.6. Where the structure is smaller than the 9T TSPC flip-flop and fewer clock transistors, therefore, it

is not used by simulations. The main reason is in this structure some nodes are not fully implemented for VDD or GND.

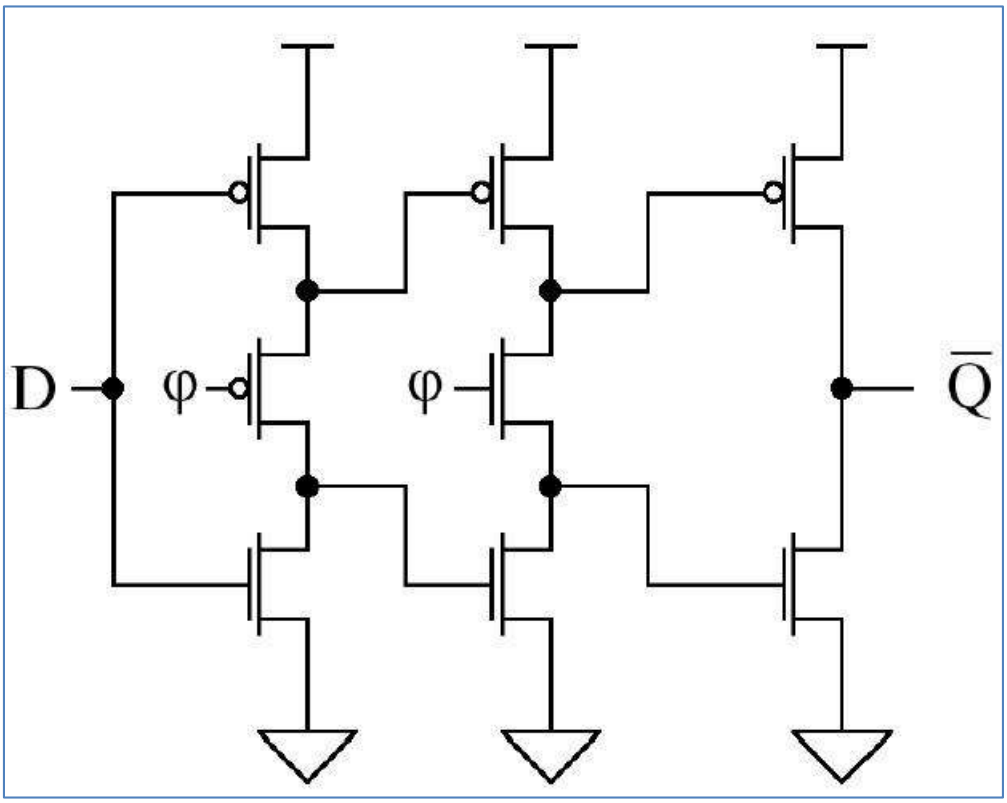


Figure 2.7 8T TSPC flip-flop

2.5.5 Hybrid latch flip-flop (HLFF)

This system is based on a sharp pulse on the positive edge of the clock using a clock and late clock with a sharp pulse (Partovi *et al.* 1996) locally based on a sensitive latch. This Hybrid latch Flip-Flop (HLFF) is shown in Figure 2.8.

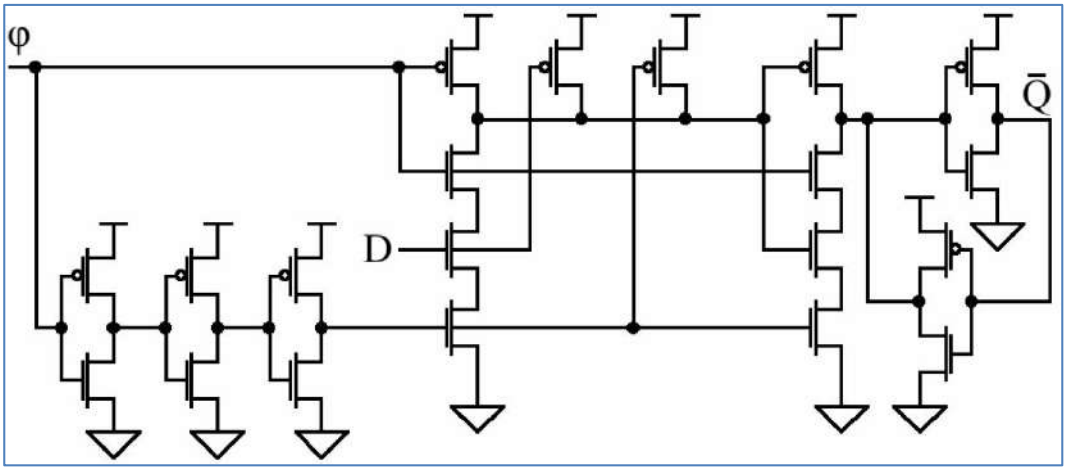


Figure 2.8 Hybrid latch flip-flop (HLFF)

2.5.6 Semi-dynamic flip-flop (SDFF)

Likewise, the Semi-Dynamic Flip-Flop as shown in Figure 2.9, the hybrid-latch and the torque-triggered Flip-Flops are also categorized (Class 1998). The delicate latch and the signal generator are the two primary construction pillars of this Flip Flop. The clock is produced from the inside of the latch by a strong pulse, so that it turns off when the signal length is too brief.

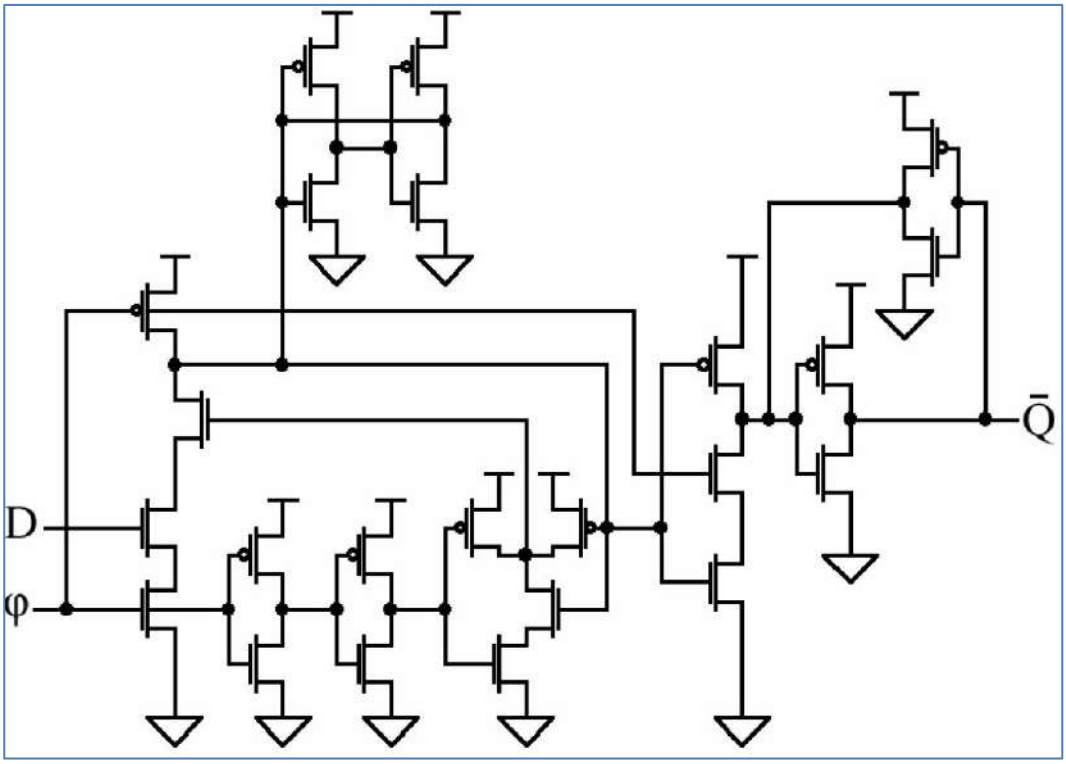


Figure 2.9 Semi-dynamic flip-flop (SDFF)

2.5.7 NAND-NOR master-slave flip-flop (NAND NOR)

NAND NOR gate is used for a single clock and two gated MS (master and slave) Flip Flops (weste *et al.* 1994, Uyemura 1992). Flip-Flop's Gate level diagram is shown in Figure 2.10. In this gate, the each and every MS latch requires 14 transistors. This flip-flop transistor diagram is shown in Figure 2.11.

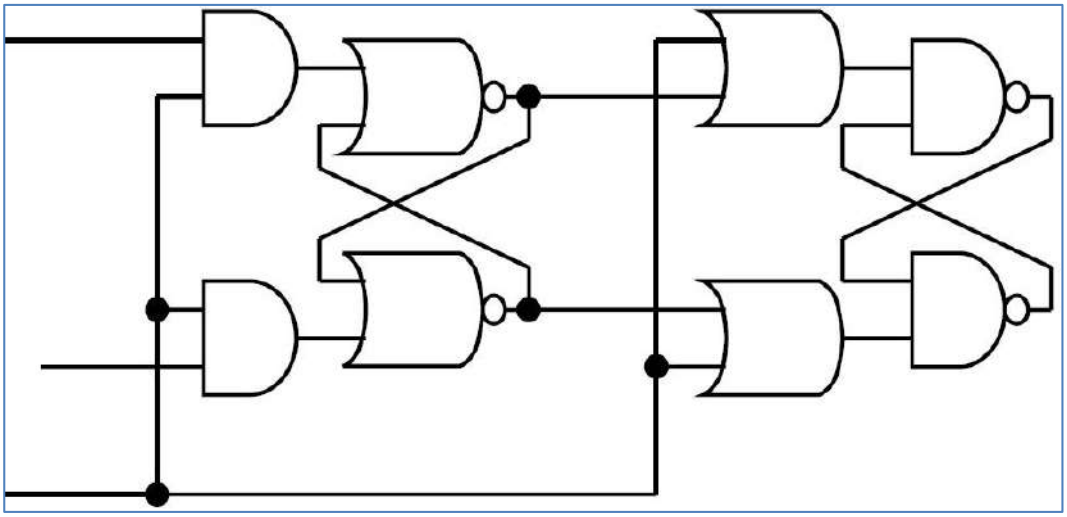


Figure 2.10 NAND NOR flip-flop

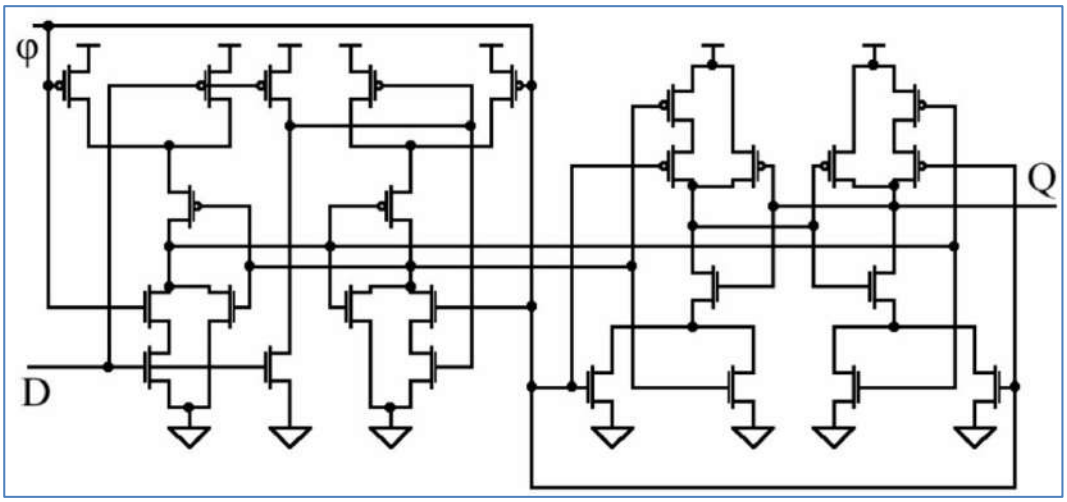


Figure 2.11 NAND NOR flip-flop (Transistor Diagram)

2.6 FLIP FLOPS DESIGN FOR LOW POWER CONSUMPTION

In that period, at the time of implementation of digital systems, the pass-transistor logic networks can give detailed considerations and emphasis to that system. Many small-swing clocking schemes are proposed to minimize the power consumption in clock distribution networks and their ability to implement practical applications (Kojima *et al.* 1999) are displayed. The prior semi-swing system needs the four clock signal and these are impacted by

skewing issues, and extra chip region is required (Kojima *et al.* 1999). The reduced clock-swing Flip Flop (RCSFF) is used to decrease spillage (Kawaguchi and Sakurai 1998) for elevated power supply voltage. For half-swing watches, a single-clock Flip-Flop requires not a high voltage but has a lengthy latency (Kwon *et al.* 1999).

Also called the simplest FFs are the Hybrid-Latch Flip-Flop (HLFF) and Semi-Dynamic Flip-Flop (SDFF). However, these two flip-flops consumes a large amount of current because of the redundant transitions at internal nodes (Partovi *et al.* 1996 and Klass 1998). To overcome this problem, the authors (Kong *et al.* 2000, Stojanovic and Oklobdzija 1999) proposed a Conditional Capture Flip-Flop. Although, the HLFF, SDFF, and CCFF are used in full-swing clock signals, which cause significant power consumption. This research focuses only on the creation of an embedded device that modifies internal features by means of distinct pass transistor (PTL) logic. Pass Transistor Logic is an excellent route to create a lower-power loop.

The paper (Esmaeili *et al.* 2010) said that about conditional capture method. This method is mainly used for minimizing the power consumption in low data transfers by eliminating redundant internal transition. This method is done by reducing short power of the loop. In decreased swing inverters, the grid pMOS transistor is always saturated since Vgs = Vds is always enhanced by the voltage of each pMOS source on each network VDD- | Vtp | This leads to the low-swing sinusoidal clock signal in the lowest cycle and its peak voltage.

The paper (Esmaeili, *et al.* 2010) said that differences on the results obtained from the definitive and post-layout simulations for the double edge-triggered flip-flop. The modulated sinusoidal clock wave transforms into a square wave clock when a power supply transforms upright. Effect of the

useful edge of the CLK1 sinusoidal motor output used to describe the first TE1 range and then compared with CLK2, which is used to define the second assessment interval of TE2. Also, on the TDQ delay against TDCLK delays are compared with the short-term effect of the inverse square signal CLK2.

The paper (Kim *et al.* 2002), and an IEEE affiliate, these two individuals are developing a plan for our LSDFF which uses the front end information selection and the rear side of the data transmission. The X and Y are loaded and issued from the inner nodes depending on the entry information Din, but are served by the clock wave. The only inner nodes of LSDFF are altered after the entry has been altered. The LSDFF can use a single-phase (TSPC) Flip-Flop and does not involve a conditional catch system. The PTTFF is one of the data-precharged internodes, which can affect the flip-flop. Moreover, there is no full voltage swing at its internal nodes, which causes performance degradation.

These two individuals (Hamid Mahmoodi *et al.* 2004) design standard Flip-Flop-clocked power rehabilitation. This flip-flop contains a four-phase (FPTG) transmitting gate. The FPTG is identical to the traditional Transmission Gate Flip-Flop (TGFF), apart from the four-transistor pass-gates that are engineered to be operated during short time frames. The primary disadvantage of this Flip-Flop is that four sinusoidal clock inputs and long distances are needed. The gates are very big transistors needed and produce the outcome in big Flip Flop regions.

The paper (Chen *et al.* 1998), focused on using power transistor stacking method for leakage reduction. The stacking threshold current decreases highly and it also reduces the DIBL effect. In result of above work, it also reduces the sub threshold leakage. (Tsividis 1987) used Voltage hopping circuit for decreasing subthreshold current. A control signal is used to

guide the voltage-supply where it is linked to MOS device to control the low and high voltage based on the operations. (Chung *et al.* 2001) discussed about various kinds of dual-edge triggered FF and suggested a best DETFF based on the best performance for digital operations. (Pedram *et al.* 1998) stated that, clock gating circuit is also one the methodology which can reduce the power consumption. The unnecessary switching method is eliminated by the clock gating in the node of the circuit. The author insisted that the input of D-FF is same to its output hence it can control the clock, triggering of D-FF through which the power consumption can be reduced. (Nedovic *et al.* 2001) stated that the period of clock time is very crucial for any sequential circuits. Similarly, setting and holding time is time-limited for the input. Whereas the propagation delay of any device needs to be lesser than the clock time. Like various limitations are related to clock and data time need to be considered. Also, the authors (A.P. Chandrakasan *et al.* 1995), (Sanchez-Sinencio *et al.* 1999), (Rabaey and Pedram 2000), (Chandrakasan *et al.* 2001), (Kiat-Seng *et al.* 2009), (Shoji 1992), and (Tsividis 1987) have been discussed about various types circuit designing method for low power and high speed applications based on the CMOS specifications.

Two pass-transistors are used mainly in the circuit design such as NMOS and PMOS. NMOS is used in CPL, (Yano *et al.* 1990) and PMOS is used in DPL (Suzuki *et al.* 1993) and in DVL, (Oklobdz *et al.* 1995). Complementary pass-transistor circuit in (Yano *et al.* 1990) used both NMOS in input and CMOS in output. These grids are a tree prototype and have pull-down and pull-up roots. The NMOS frequency drop deteriorates the elevated performance amount of the CMOS inverter. In, (Yano *et al.* 1990), Abu-Khater *et al.* (1996), Cheung *et al.* (1997), the CPL has been used for arithmetic building blocks and it provides high-speed in operations with diminished transistor count.

Another factor considered in the above designs is noise, which need to be reduced in CPL. So, two PMOS transistors are added as branches in the N-tree of DPL, (Suzuki *et al.* 1993). It increases the input capacitances, though the two transistors increase the load for increasing the speed. But the full-swing process enhances the performance of the circuit for decreased voltage supply and restricted voltage level.

One of the major disadvantages in DPL is redundancy. It needs a greater number of transistors which is actually higher than the required number for realization of a process. In order to overcome the problems due to redundancy a novel logic group, DVL, (Oklobdz *et al.* 1995), is created from the DVL. It conserves the occupied swing process of DPL by means of decreased transistor count. In (Oklobdz *et al.* 1995), proposed a new DVL circuit which has been can be created from DPL circuits.

2.7 SENSE AMPLIFIER FLIP FLOP

The latching elements have been imposed on number of clocking formats with limitations by the digital structure to conclude their usage in various systems. Frequently employed schemes were single phase and dual phase clocking. The investigation on the time involvement in synchronous digital schemes was exhibited elaborately in the work (Abu-Khater *et al.* 1996). A contrast investigation between the flip-flops and latch applications in highly performing systems was completed and published in research works (Chandrakashan *et al*. 2000) and (Esmaeili *et al.* 2009). This evaluation was the trade-offs between the velocity, power and time setup on the time sequence of the system.

With the nature of low power consumption and appropriate time restrictions, timer devices, latches and flip-flops were involved in the digital

systems. In the high-performance systems, the clock generating arrangement loading is primary as it consumes a major portion of the total power consumption in the total system which was explained in (Esamaeili *et al.* 2010). For better performance, short network setup and hold time is more essential, that is mostly disregarded. During the experiment and analytic process, the information from the Flip Flops within and outside of the system has to be recorded in a multifaceted arrangement.

The number of logic levels between the channel phases has to be reduced as the frequency increases that some part of the logic has to be entrenched in the Flip Flops. In the minimum cycle times, the clock skew increases in depth in the micrometre designs, where it doesn't follow the technical scaling meanwhile and the absorption of clock skew in a stipulated time is much more significant (Kawaguchi *et al.* 1997). This supplement requisites forced on the latches has to be given equal significance with their performance characteristics. The total time taken from the device is the addition of erection time and the clock to output delay.

The time elapses between the last point of data arrival and the yield conversion measures the device delay time. Intrinsic parallelism is revealed in the cavernous channel system, which entail vast fan out in the output of the register. With superior driving strengths, the devices can be operated with minimum delay time, examples can be represented with the Sense-Amplifier-based Flip-Flop (SAFF) investigated in (Cooke *et al.* 2003), Hybrid-Latch Flip-Flop (HLFF) investigated under (Fuse *et al.*2001) and SDFF proposed in (Hesley *et al.* 1999, Hu *et al.* 2007) As SAFF is restricted by the latter ones, due to its limitation in erecting the output latch.

2.8 A SURVEY ON POWER DISSIPATION METHODS

Some of the methods used for power dissipation by concentrating on static and dynamic power variations and these are the two major components determine the total power dissipation. Several methods used for designing a circuit for low power and high-speed applications in VLSI field. Some of the methods are better for static power dissipation than dynamic power dissipation. Some of the methods used for reducing the power leakage to reduce the power dissipation are:

1. Transistor stacking [Chen *et al.* (1998)]
2. Multi Voltage technique [Mutoh *et al.* (1995)]
3. Dynamic Voltage technique [Koichi Nose *et al.* (2002)]
4. Scaling of supply voltage [Fuse *et al.* (2001)]

Some of the methods used for reducing the dynamic power dissipation are:

1. Supply voltage scaling [Rabaey *et al.* (2000)]
2. Node capacitance reduction [Chandrakashan, (1992)]
3. Reduction in frequency [Chandrakasan *et al.* (2001)]
4. Reduction in switching activity [Chandrakasan *et al.* (2001)]

From the above discussions it is identified that each technology embedded in the design and portions included in the conventional FF design improves the performance in their own way. Hence by incorporating various logic functions and circuits can increase the efficiency of the FF circuit in terms of power consumption, delay, area and speed.

2.9 SUMMARY

This chapter presents the Flip Flops design methods with various topologies. It is also explores various kind of Flip Flop circuits designs with the diagram. One of the major portions is topologies of Flip Flop designs which provide better knowledge about the Flip Flop circuit system. This chapter discussed about energy and delay-based Flip Flops for high performance systems. The set of all Flip Flop discussed have been designed in standard 0.13μm CMOS technology at 1.2V. Also, from the simulation and experimental results it is very clear that the performance need to improve for present and future VLSI applications.

CHAPTER 3

EXISTING APPROACHES

3.1 OBJECTIVE

This chapter presents the various existing approaches used in this research work for obtaining the issues and challenges of earlier research works and evaluating the performance of the proposed approaches. It presents the detailed information about the design and circuit method for dual edge triggered Flip Flop and sense amplified dual edge triggered Flip Flop. From these Flip Flops, it is easy to understand the proposed modified dual edge triggered sense amplified Flip Flop and identify the better performance.

3.2 EXISTING APPROACHES

A new open-pulsed dual-edge triggered Flip-Flop for limited-power and elevated-performance application were initiated in this study. The DET-SAFF can also attain low-power usage with a tiny pause by integrating the dual-end ignition system in a fresh quick button and using contingent pre-charging. A clock-based sensory amplifier is used to further decrease power usage in small changing operations. A comprehensive post-layout analysis has illustrated that the suggested DET-SAFF has both low-and elevated-speed features, with a time and energy decrease of up to 43.3% and 33.5% successively. If the changing operation is less than 0.5, the suggested CG-SAFF shows its supremacy in the decrease of energy. CG-SAFF can save up to 86% of energy during the null entry changing operation. This study has lead Modified Clock Gated Dual Edge Triggered Sense Amplifier Flip-Flop (MCGDET-SAFF) to raise the energy and error decrease proportion.

While thinking about the low power design circuits, the power dissipation occurs in the digital circuits due to any one of the occurrences like switching the circuit in any short circuits, leakage of power and also due to power consumption in static devices. Almost 90% of the power is consumed during switching which may vary according to the clock frequency and number of transistors in the circuit. The parameters to be considered while designing a Flip Flop includes the output delay with small clock pulse constricted sampling window, higher driving capability and lower clock load with low power utilization. In a 0.18µm CMOS Flip Flop (FF) circuit has a load in a range of 50fF to over 200fF. The power consumption of Flip Flop includes the power consumption in internal circuits, data power and by clock circuits. The two types of power dissipation in a CMOS circuit are static and dynamic power dissipation

Sub-threshold, gate current leakage and leakage due to reverse biased diodes and conflict current results in the static power dissipation and capacitor switching, shorting in circuits and leakages in gate circuit results in dynamic dissipation of power. If the frequency of the clock is reduced, power also reduced. Short circuit current is of low value compared to switching current, which is forced by direct short circuit. The fabrication decides the level of leakage power. In VLSI technology, power reduction plays a vital role to extend the battery life and reduces the usage of natural resources resulting in better system reliability.

In pulse triggered Flip Flops, implicit pulse generator is utilized for implicit pulse triggered Flip Flop and an explicit pulse generator is used in explicit pulse triggered Flip Flop for generating the clock pulses. In implicit pulse FF, the pulse is produced by the internal pulse generator. So that, other Flip Flops couldn’t use the same whereas in explicit FF, an external pulse generator is used that can be shared to the neighbouring Flip Flops. This can

be attained by implementing lesser number of transistors when compared to internal pulse generator circuit. To reduce the gate power consumption, various combinations of logic gates were used in gate circuit design.

A pulse generator mainly finds their applications in electronic design circuits that create rectangular pulses for working in digital and as function generators in analog circuits. These circuits used to drive the devices like switches, optical components, laser applications, in modulator circuits. Pulses with variable frequencies can be generated and applied to digital circuits. They are most suitable for the circuits which need low distortion and non-variable signal frequencies

3.2.1 Flip-Flop with Sensing Amplifier

The block diagram illustrates the operation of Flip Flop which is discriminated from the master slave (MS) which has a combination of two parallel latches. If it is not assured with suitable margin between two phases of clock, the MS pair will be translucent. The unit comprises of two parts called signal processor and slave lock comparable to the MS device's master and slave latches. The functional output of the data and clock signal is the primary stage in the structure. If there is variation in the data and clock signal output, the pulses with different width can be yielded which sets slave latch. The later stage is sensitive to the clock transition (From 0 to 1 or 1 to 0) and not to the level as in MS grouping. The flexibility and quality of the function of they may be endangered sometimes due to the sensitive implementation of Pulse Generator level.

Due to this risk level in the employment of Flip Flops, it has been avoided in a few methodologies like LSSD of IBM (IBM- Manual 1985).

The sense amplifier holds the first level and slave, set, reset, clock to the second level. The general structure of a flip-flop is shown in Figure 3.1.

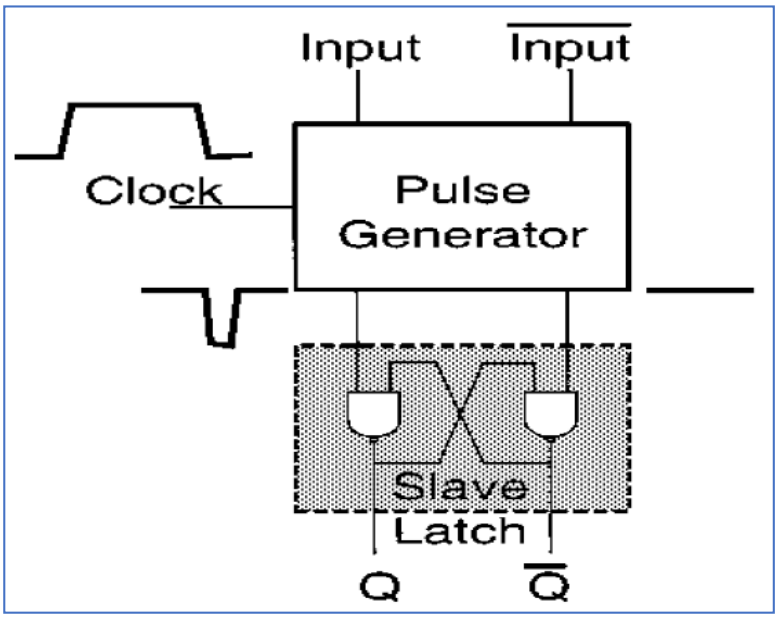


Figure 3.1 General structure of a flip-flop.

An adverse pulse is supplied to the slave panel terminal according to the yield needed to be updated or configured. As illustrated in (Madden and Bowhill 1990) and (Kobayashi *et al.* 1993), SA is a pulse producing module in this SAFF Flip Flop. This sense the real and discrepancies in the inputs. Tracking the leading clock edge, a monotonic variation from high to low level in any one of the outputs was generated by the SA stage. The output of SA will not be influenced even if there is any disparity in the data clock intervals. Unless the next leading edge prevails, the SA latch holds the state and won't leave for any transition. The two outputs of this module reach high level once the clock shifts to inactive mode which leaves the module to proceed as Flip Flop. The SAFF is shown in Figure 3.2.

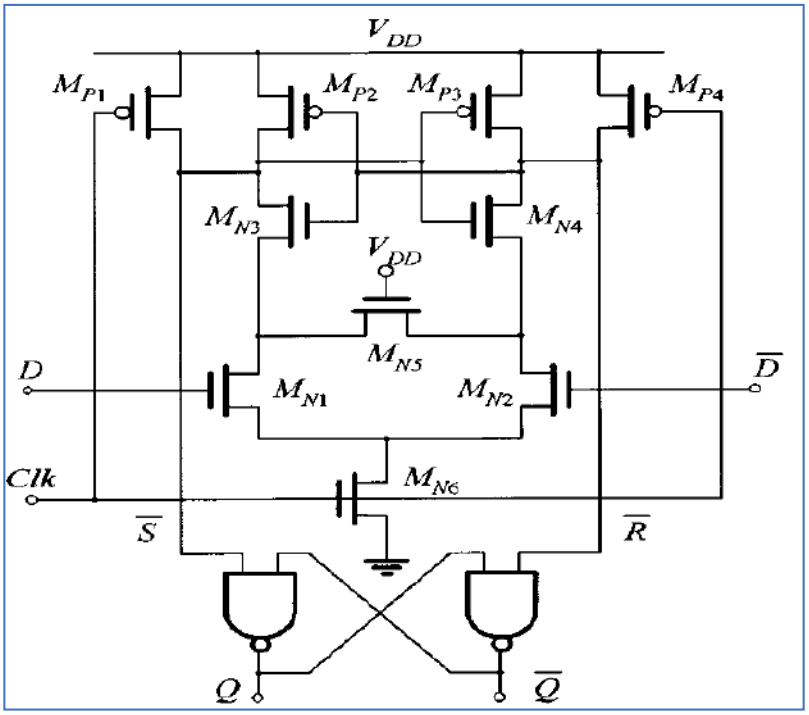


Figure 3.2 SAFF [M. Matsui *et al.* (1994)].

3.2.2 Design of Dual Edge Triggered Flip-Flop

In the dual edge triggered Flip Flop, the input data is transferred to the output end during the rising edge and trailing edge of the clock signal. Number of assessments has been encountered to achieve this as DETFF, by cascading the positive and negative edge triggering devices and engaging them with conflicting clock phases as illustrated below in Figure 3.3. In this work, an advanced DETFF is proposed to yield a better result than previous one. Here, initially a petite duration pulse is created at the edges of clock, and that pulse is to trigger the transmission gate connected to input data. A latch is connected at the output end to accumulate and store the contents which may be used for the error correction

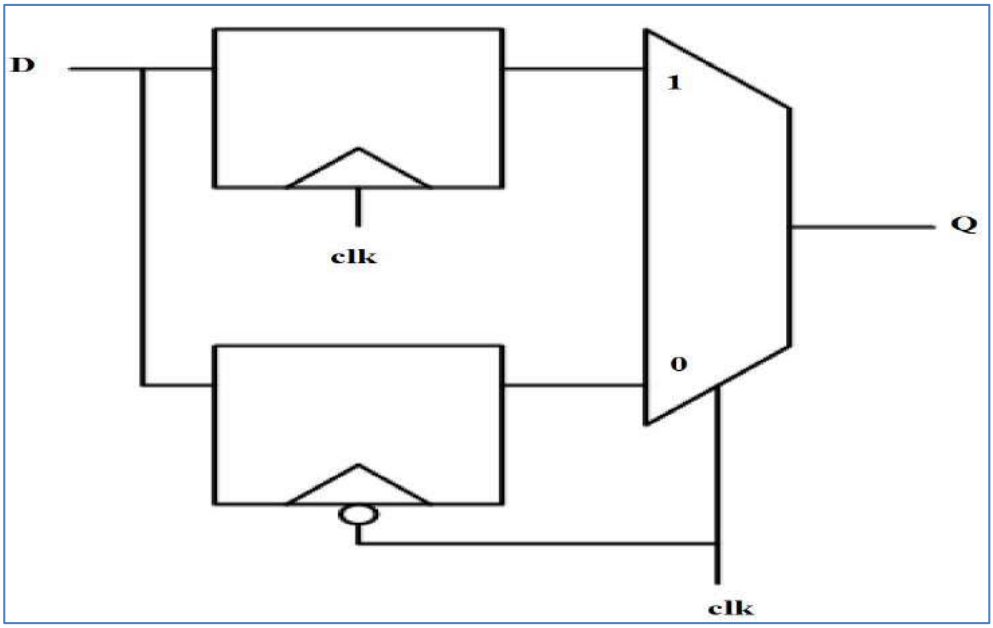


Figure 3.3 Simplest way to make DETFF

The pulse producing circuit holds delay creator network in which quadruple (four) inverters coupled serially. Also consists of a XNOR/XOR logic circuit to yield differential outputs from the circuit. The illustration of the working of DETFF with blocks is depicted in Figure 3.4.

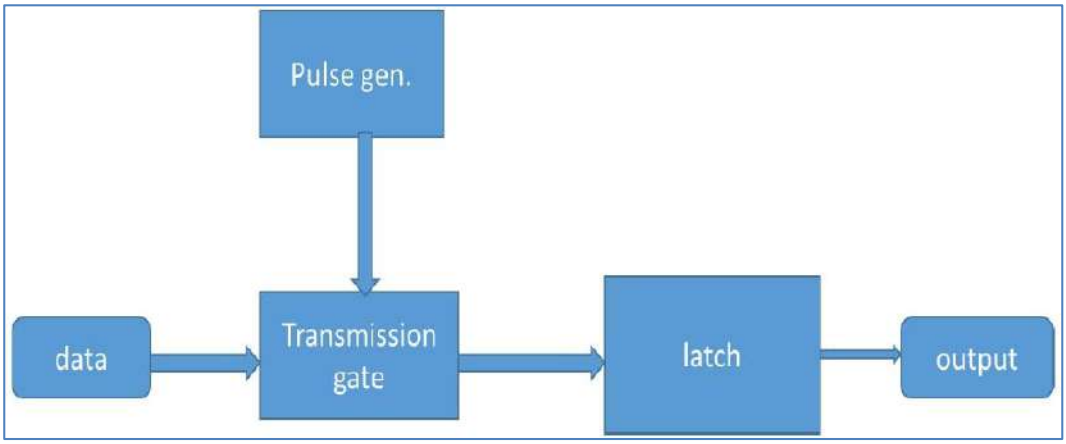


Figure 3.4 Block diagram for DETFF

3.2.3 Traditional DETFF

The circuit diagram in Figure 3.5 shows the normal DETFF which induces the regular results with large propagation delay.

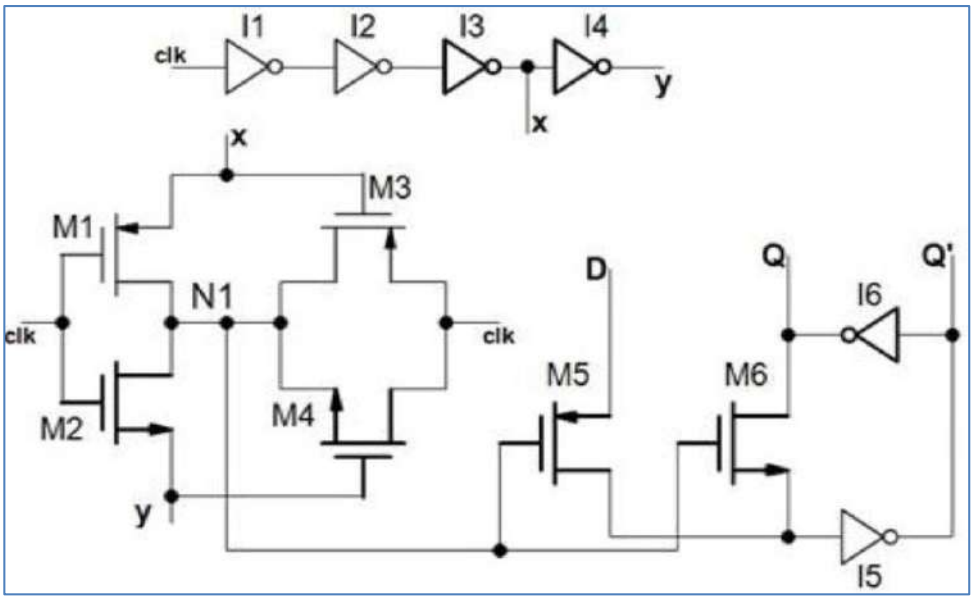


Figure 3.5 Schematic of conventional DETFF

The I1, I2, I3, I4 are inverters that yields a clock pulse with a delay. Let an inverter has a propagation time delay of τ_i seconds, this tilts the input propagation delay time by $4\tau_i$ seconds. From the Figure 3.5, Signal y and signal x will be a tilted form input pulse with a delay time of $3\tau_i$ seconds.

Inverter I3 and I4 have superior threshold values of voltage. MOSFETS are connected in such a way that N1 = clk ⊙ y, shown in Figure 3.6, when the pulse changes over from low to high, M2 is triggered to produce a output to N1, M1 is turned off, MOSFET 3 will be turned on by a delay of $3\tau_i$ and M4 will turn on by a delay of $4\tau_i$. The terminal N1 liberates through M2 for a period of $4\tau_i$, as signal y = clk $(t-4\tau_i)$, beyond that time delay, N1 gains charge from M1 and M4.

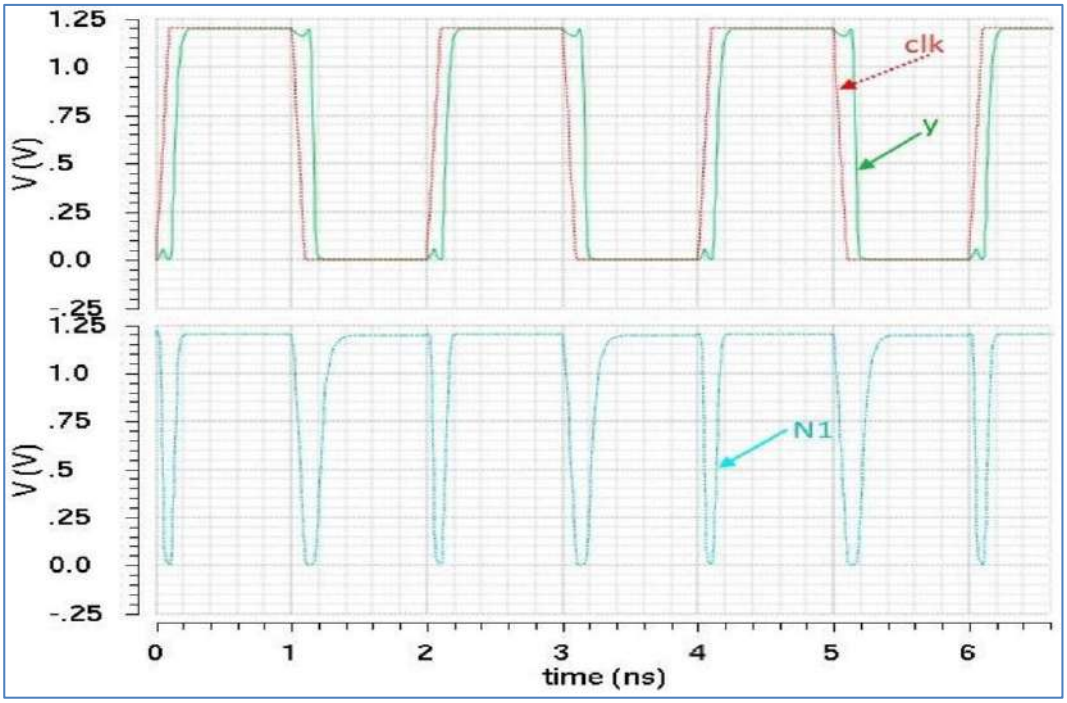


Figure 3.6 N1 = clk⊙ y

Similarly, when the clock pulse transits from high to low, MOSFET M1 gets triggered, M2 switched off, M3 turns off by a time delay of $3\tau_i$ and, with a time delay $4\tau_i$, M4 will be turned off. In a delay period of $4\tau_i$, N1 discharges all the way through M1, M3, and M4. After the specified period N1 gains charge by MOSFETs M2 and M3. To afford a stable output in logic levels, all of those MOSFETs (M1, M2, M3, and M4) has been combined. The XNOR output is exhibited in-between clk signal and the output y.

The output D is from the MOSFET M5. During the period of $4\tau_i$. N1 sustains at a low level (0) which triggers D to Q via M5 and inverters I6 and I5, and when N1 migrates to high level M5 turned off and M6 enabled resulting in latching Q output.

3.2.3.1 Recommended 2 DETFF

With simple alterations, to create a non-erroneous signal, a modified DETFF is recommended in this chapter and the logic diagram is shown in Figure 3.7. With the usage of transmission gate, the data is transmitted to the output level with a lesser propagation delay.

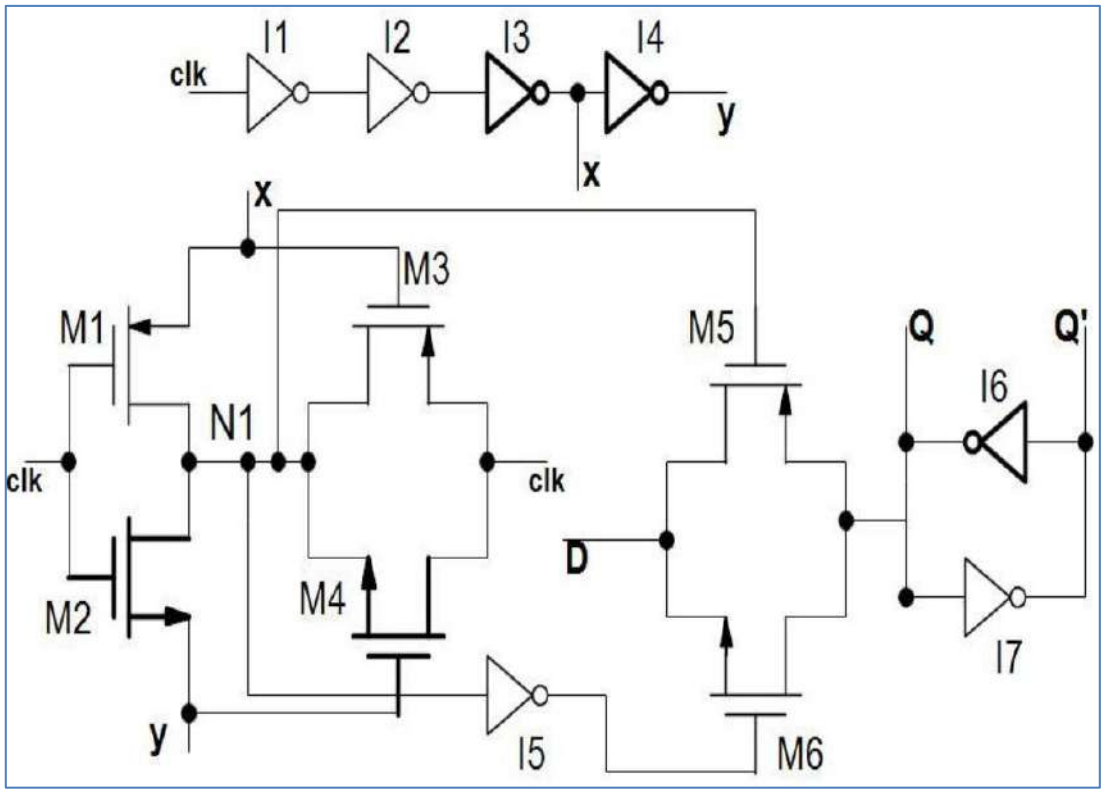


Figure 3.7 Proposed_2 DETFF

Inverter I5 is used to activate the M5 and M6 in the transmission gate. Likewise, conventional devices, the changes in N1 do not influence the data latching. The D signal is shifted to Q output when the N1 signal is at low level. Even if not, the changes in D won't affect the Q.

3.2.3.2 Recommended 1 DETFF

In this model, XOR logic is utilized to induce a spiky clock pulse. An individual inverter produces a delay time of τ_i. Four inverters I1, I2, I3, I4 were employed to produce a total delay period of $4\tau_i$. The circuit for this model is illustrated in Figure 3.8.

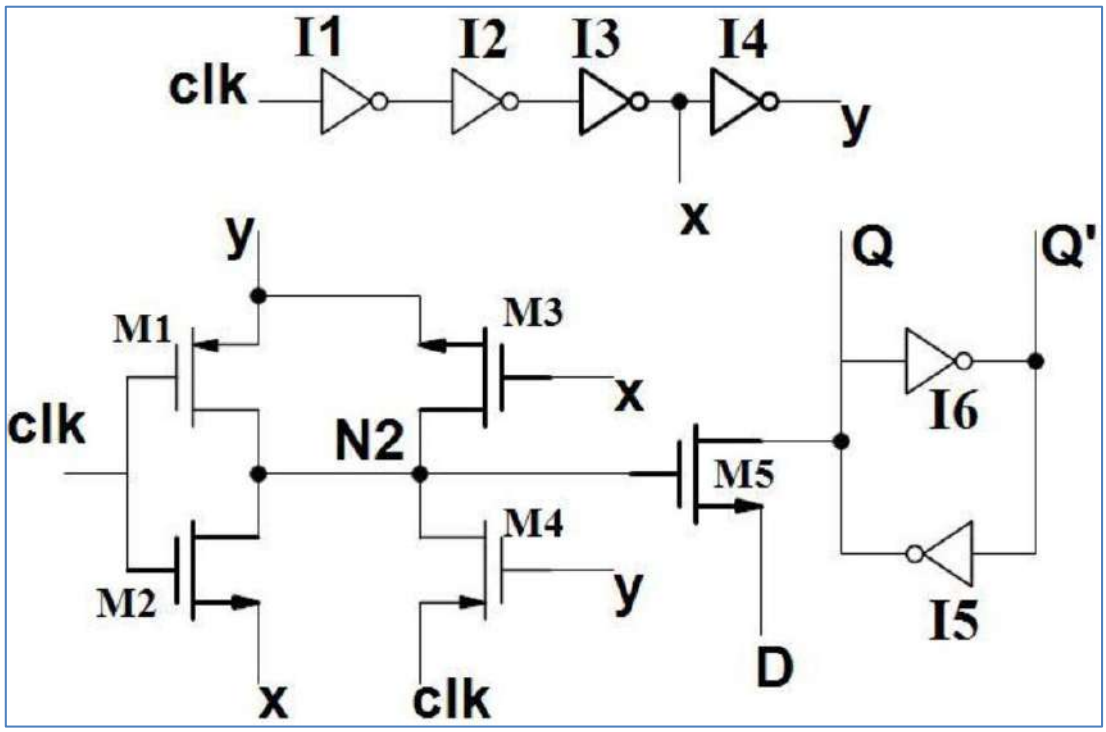


Figure 3.8 Schematic of Proposed 1 DETFF

In this, y = clk(t-$4\tau_i$) and x = clk'(t-$3\tau_i$),whenever clock modifies from low to high, M2 gets triggered resulting M1 to switch off immediately and M3 turns off with a delay time of $3\tau_i$ and M4 will be turned off by $4\tau i$. For a period of $4\tau i$, M4 charges N2 and M2 charges the device N2 by a time period of $3\tau i$. Until clock remains in the high state, M2 remains ON, charging N2 and leaving other MOSFETS in off condition. If the state changes from high to low, M2 goes off, leaving other MOS devices ON with a specified delay. Summarizing this, when clock is low, N2 gets charged by M4 for a

period of 4τi and when clock is at high level, N2 is charged by M1 for the same time period. Whenever clock remains at 0, N2 discharges through M1, M3, M4 instantly resulting N2 with sharp high edge, for the time of 4τi with the relation of N2 = clk XOR y. The result of N2 signal has been given in Figure 3.9. Until N2 remains in high state, M5 is triggered and data D gets latched to Q by I5 and I6. The variations in D will not influence the Q until clock is in low level.

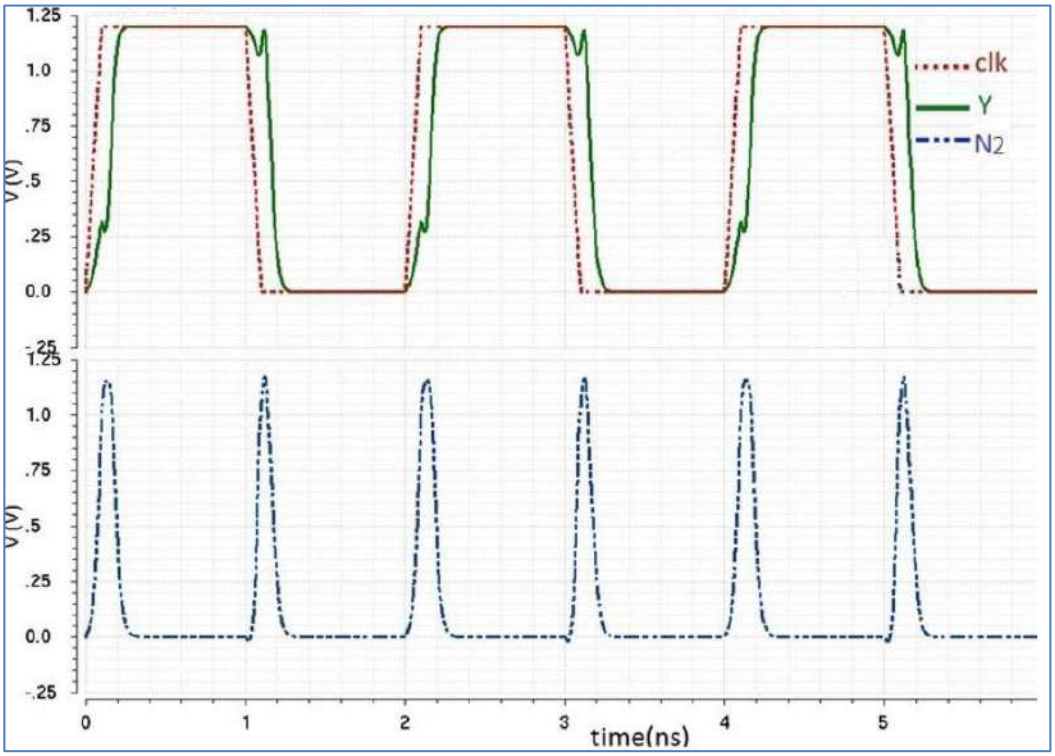


Figure 3.9 Output from node N2

3.2.4 Clock Pair Shared Flip Flop (CPS-FF)

One of the existing systems named CPS-FF is described here for evaluating the performance of the proposed Modified Clock Gated Sense Amplifier Flip Flop (MCGCA-FF). In the CPS-FF clocking transistors used in the VLSI design is very less which reduces power consumption with less area. CPS-FF comprises of low swing differential conditional capturing Flip Flop

for performing low swing sinusoidal clock where it reduces inverters used in the clock port. The low swing clocking basically need two voltage levels for dual supply voltage and regular power supply schemes. The dual supply voltage includes more circuit with additional area in the overall chip design and increase complexity. In addition to the CPS-FF it is very easy to create a dual edge Flip Flop using a simple clocking structure also CPS-FF can be used as a level convertor Flip Flop due to the data signals only drive in NMOS transistors and incoming clock. In CPS-FF due to the floating values and high swing are produced at the same time the output cannot be obtained properly. Because the clock input is a square wave there will be a high swing output in the circuit, so an inverter stage circuit is used to overcome the disadvantage and additional modifications is applied. Hence an LSDC-FF is proposed by sending a sine wave as an input where it reduces high swing output. In addition to this the number of transistor count is minimized using modified pass transistor logic in CPS-FF, where it reduces the power consumption. In the existing design approaches, there are two pass transistor circuits are used such as NMOS and PMOS.

NMOS is used in CPL, (Yano *et al.* 1990) and PMOS is used in DPL, (Suzuki *et al.* 1993) and in DVL, (Oklobdz *et al.* 1995). Complementary pass-transistor circuit in (Yano *et al.* 1990) used both NMOS in input and CMOS in output. These loops are intended as a model of a tree and have both draw-down and draw-up branches. The NMOS frequency fall deteriorates the elevated performance amount of CMOS inverters. In, (Yano *et al.* 1990), (Abu-Khater *et al.* 1996), & (Cheung *et al.* 1997), the CPL has been used for arithmetic building blocks and it provides high-speed in operations with diminished transistor count.

Another factor considered in the above designs are noise, which need to be reduced in CPL. So, two PMOS transistors are added as branches in

the N-tree of DPL, (Suzuki *et al.* 1993). It increases the input capacitances, though the two transistors increase the load for increasing the speed. But the full-swing process enhances the performance of the circuit for decreased voltage supply and restricted voltage level.

One of the major disadvantages in DPL is redundancy. It needs a greater number of transistors which is actually higher than the required number for realization of a process. In order to overcome the problems due to redundancy a novel logic group, DVL, (Oklobdz *et al.* 1995), is created from the DVL. It conserves the occupied swing process of DPL by means of decreased transistor count. In (Oklobdz *et al.* 1995), proposed a new DVL circuit can be created from DPL circuits.

3.2.5 Dual Edge Triggered Sense Amplifier Flip Flop Design for Low Power Applications

The energy discharge is caused by four causes in digital circuits like shifting energy, short-circuit control, leak control and dynamic control. To change the unit by 90% of the complete energy needed, the amount of integrated circuits and the operating rate are also determined. Tiny Clk-output lags, narrow screen sampling, poor energy, small clock charge, high operating capacity are needed in the Flip-Flop Design. Typical 0.18 μm CMOS technology Flip Flop load ranks between 50fF and more than 200fF in critical routes and typical values of 100-150fF. The total Flip-Flop strength is evaluated as inner energy, information capacity and clock capacity. CMOS control dispersion is of two kinds: static and vibrant dispersion. Sub threshold, present leakage, inverted diode leakage and the contention flow are included in the static dispersion of energy and owing to capacitive transitioning, short track or port of Leakage, vibrant energy dissipations. When the clock rate is decreased, the energy is decreased. The shortened loop strength, as opposed to

the changing energy, is vibrant and is powered from the short circuit guide. The strength of the spill is decided by the technology produced. The VLSI power decreases the life of the battery, expenses, utilization of valuable resources and maintenance of the scheme.

One internal Flip-Flop is caused by a pulse, wherein the internal signal generator is used to generate the clock pulse, and a second is the Flip-Flop explicitly caused by an impulsive pulse wherein the pulse produced by an external signal generator method is used. The clock pulse within the tapered pulse cannot thus be used throughout the full loop by the neighbouring tapered pulses. The signal is produced internally by the signal generator with specific Flip-Flop pulse. The signal generator can be distributed by the next Flip-Flop in this form of Flip-Flop, the technology that does not use the explicit pulse of the Flip-Flop. In this case, the proportion of integrated circuits is reduced compared with the inner Flip Flop form signal generator. Different combinations of logical gates can create the same circuit performance with various power consuming values in the gate design of the system.

3.2.6 Sense Amplifier Based Flip-Flop

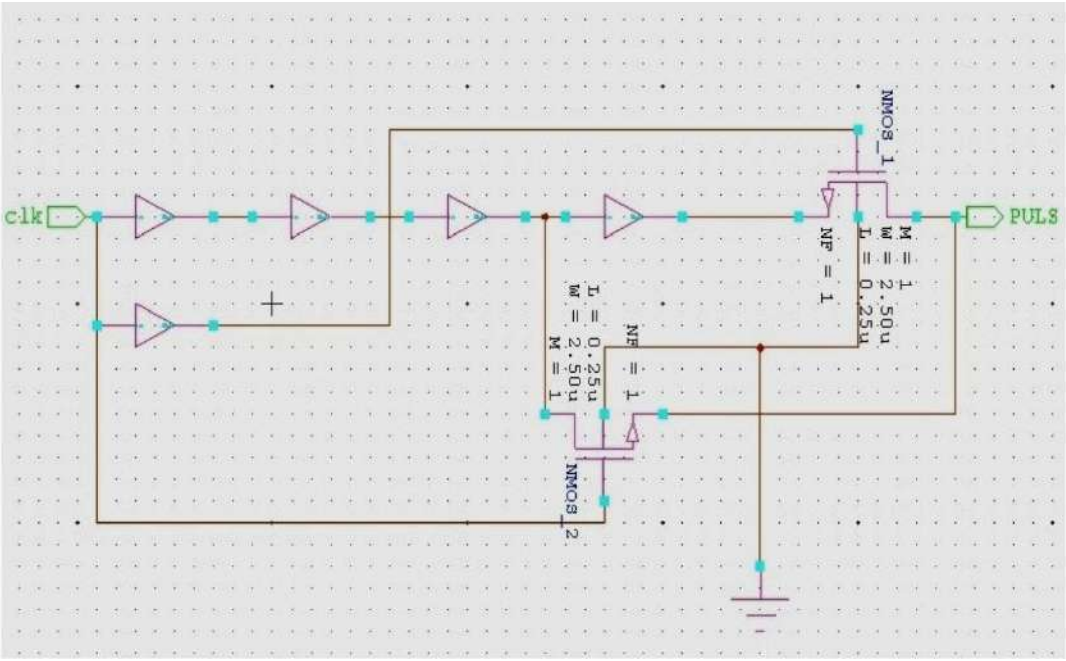
Cross-coupling NAND Speed limiting factor is the sensory-based Flip-Flop circuit (SAFF). Also called the SR latch that is active during production. It is a cross-connected settings button. The fresh Flip Flop utilizes a fresh topology of the input phase, which decreases delays significantly and increases mobility. The sensor module has a lower construction percentage, decreased energy dispersion in short-circuit and free activity without glitches. (Nikolic *et al.* 2000) has proposed it. With a symmetric slave latch of two inverters and two complicated CMOS gates, the SAFF has enhanced efficiency. The rise in efficiency is compensated for by increasing the number

of transistors in the production phase consisting of 16 MOS units. The sensory amplifier phase can also be used as latch whose sample gate ends when the phase changes. The device is therefore able to switch on the loop size separately. Moreover, the Sensory amplifier-based Flip-Flop (SAFF) is defined by a close-zero setting up moment, a decreased holding period and a lower clock load.

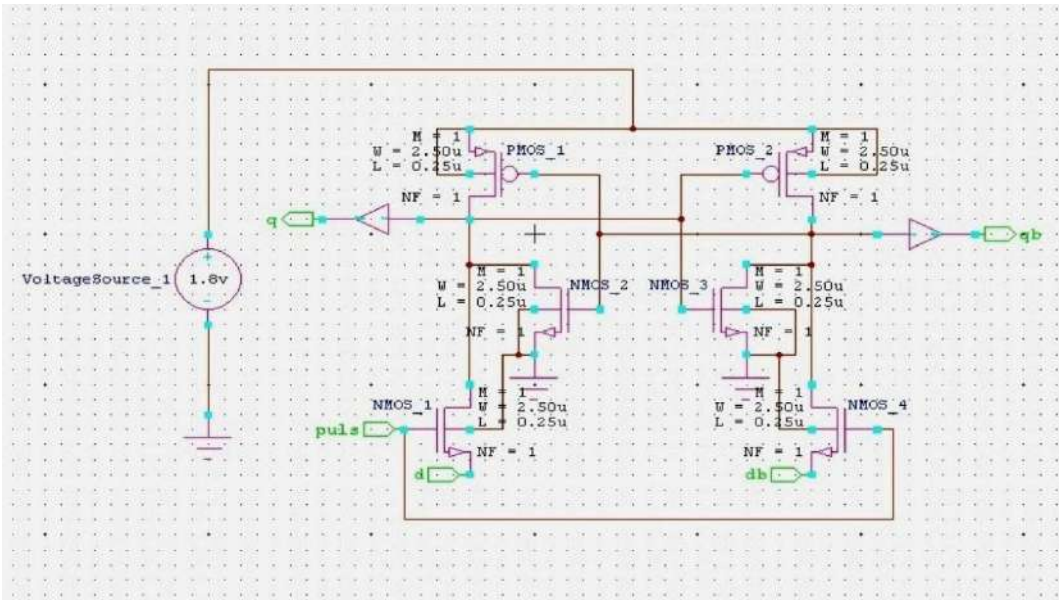
These features that construct the SAFFs are excellent options to replace normal flip-flops in normal cells. The SAFF has certain inconveniences. First, the glitching on the yield cores is more pronounced for medium load circumstances. The second inconvenience is that the use of cross-referenced inverter latches which require a right unit size unit and are subject to a crow-bar flow which improves the dispersion of energy. A disadvantage of the standard NAND-based SAFF is that the time to exit is large because of the speedy yield button. The literature has suggested to produce two high-speed knot latches to create the SAFF speeds similar or greater than the HLFF and the SDFF velocity. To differentiate between SAFF and the latch-master (MS) configuration composed of two latches in sequence. It is crucial if sufficient gaps between both the loading stages are not secured, MS latch can also be clear. This Flip-Flop's signal-generating phase feels the exact and inverse variable outputs. At one of the inputs of the front clock edge the SA phase generates monotonic switches between one and null logical level. The SA production will not be changed if the information is changed during the continuous clock interval. The transfer button also maintains the state until another favourable clock edge is reached. Once the clock is reversed, the two SA inputs will logically assume one. The whole design therefore works like a Flip-Flop.

3.2.7 Dual Edge-Triggered Static-Pulse Flip-Flop

Figure 3.10 demonstrates a scheme of a Dual Edge Triggered Static Pulse Flip Flop (DSPFF) activated dual-edge schema. The four inverters are used for reversed, postponed alarm readings in their pulse generator. For NMOS transistors, the message produced applies. These measurements produce an enclosed sample screen at both the up and down clock pulses with all these two NMOS transistors. After the pulse stream is produced via the pulse generator, both N1 and N4 transistors of the stationary lock will be activated to record information from the outputs in order to discharge either SB or RB.



(a). Dual pulse generator



(b). Static latch

Figure 3.10 Dual edge-triggered static pulsed flip-flop (DSPFF)

Since DB and impulse is supplied straight to the nodes SB and RB respectively, a lower gap may occur. Both the pMOS transistors (P1 and P2, two NMOS and N2 and N3) prevent flying stations effectively. When the Flip Flop is clear and provides a totally continuous procedure, this node seems to be SB and RB. The implicit signal generator is easy and suitable for double-edge activation. By tailoring the Transistor Section Relationship symmetrical input errors carefully, the stationary characteristic of DSPFF removes unwanted changes. Due to the big capacitance inputs at SB and RB stations, the Flip Flop latency can however drop. In addition, an elevated present leakage is associated with dual-edge dynamic beam Flip (DSPFF) Flop. This is due to a high-power supply fall through a N2 or N3 transistor when it is switched off.

3.2.8 Static Output-Controlled Discharge Flip-Flop

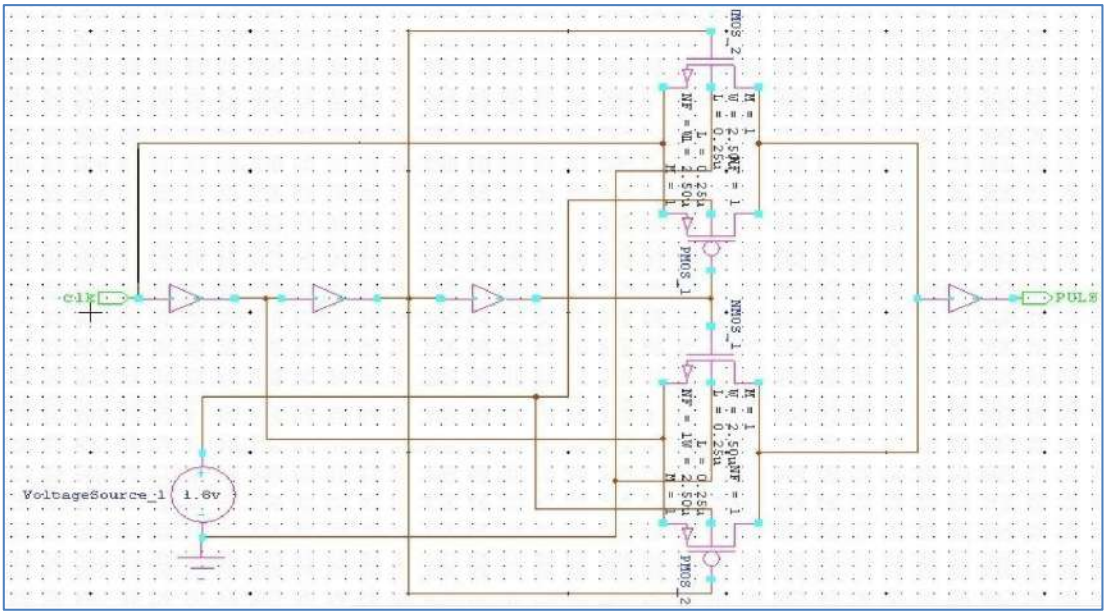
Figure 3.11 indicates a stationary outcome-controlled Flip-Flop (SCDFF) schematic diagram. Two constituent parts like the signal generator and

the Flip-Flop (SCDFF) are included in the continuous emission-controlled release. The signal generator and the pulse stream produced by the signal generator are clear. It also has a latch. The above-mentioned SCDFF latch design comprises of two stationary steps. The output quantity is shown as D. In the first step, the D input is used to control the pre-load diode to observe the X node D for the time of the sample. The retain ability technology is also used. The same is used to decrease the inner changing operations and also produces a smaller number of production failures while retaining the adverse set-up moment and short wait properties. With the conditional grab technology, the gate consumes additional electricity and the postponed clock is controlled in the flip-flop. The pre-load method was only used on implicit pulsed Flip-Flops (ip-FF), but a dual-edge activation system is difficult to employ. All such ip-FF, Flip Flops involve a bunch of transistors. For implicit and visible pulse-controlled Flip-Flops without any of the issues connected with the conditional fetch method, conditional discharge method is suggested. The additional changing function in this method is decreased by the control of the driving route when the entry is sufficiently HIGH and therefore the title Conditional download method. A NMOS QB monitored is used by the insertion of this QB on the download route which implements conditional download techniques for preventing unwanted release. Conditional discharge technology is applied so that the output stays elevated and prevents excessive discharge in node X.

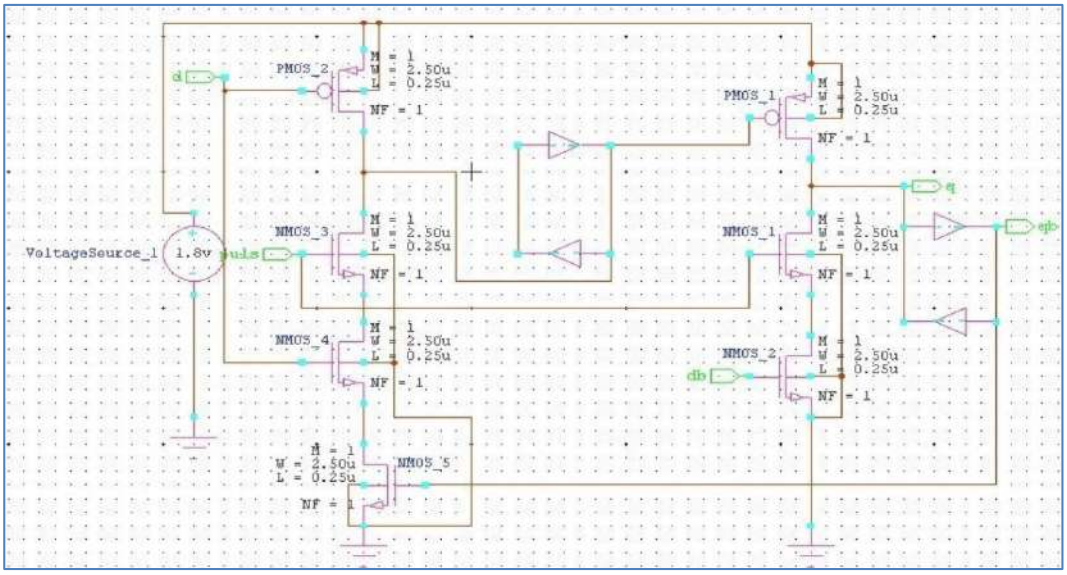
3.2.9 Adaptive Clocking Dual Edge-Triggered Sense-Amplifier Flip-Flop

Figure 3.12 shows the scheme of the Adaptive Clocking Dual Edge Triggered Sense Amplifier Flip-Flop (ACSAFF) clocking adjustable clock. Adaptive clocking dual border sensor-amplifier (ACSAFF) Flip-Flop comprises of three adaptive clocking circuit parts, front end sensor phase and Nikolic latch as illustrated by Figure 3.12. If the yield Q differs from the D

section, transistors N2 and N3 are turned into ON, CLK is provided to the rear clock signal queue. The N2 and N3 transistors are the inverter loop transistors. Node SB and RB form a release route at the dropping and rise corners of the clock signal from the front-end detection point. Transistors N4, N1, N3, N2 stop trying to charge when the output shifts. The node is also pulled down by N8 and N5, N6 and N7 at the very same moment, resulting in this N2 and N3 transistor being switched off and the inverter loop is disabled. If the information shifting operation is small, the flexible clocking inverter chains used to deactivate an inner node by transistor.

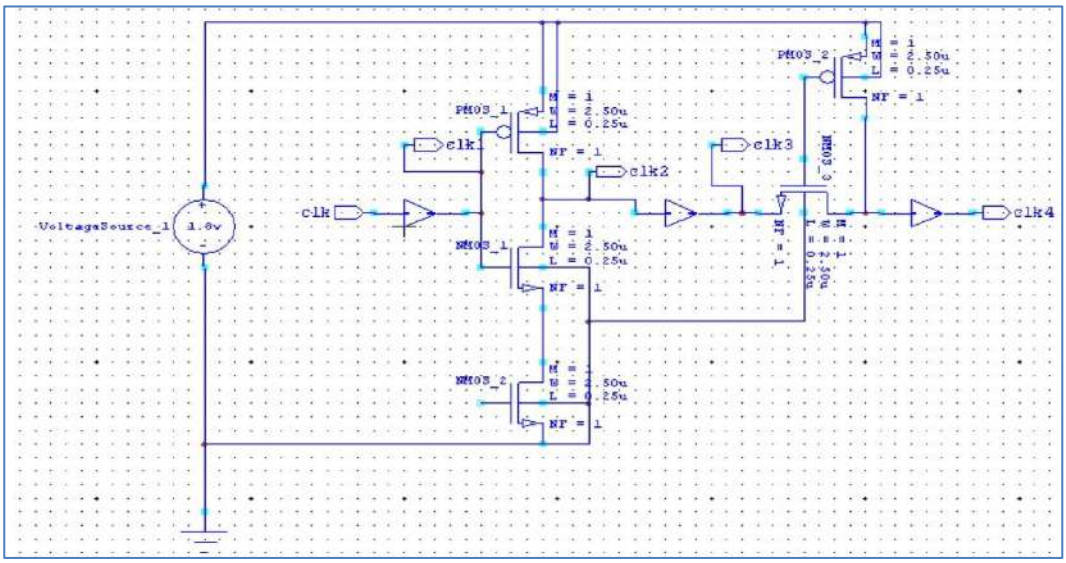


(a). dual pulse generator

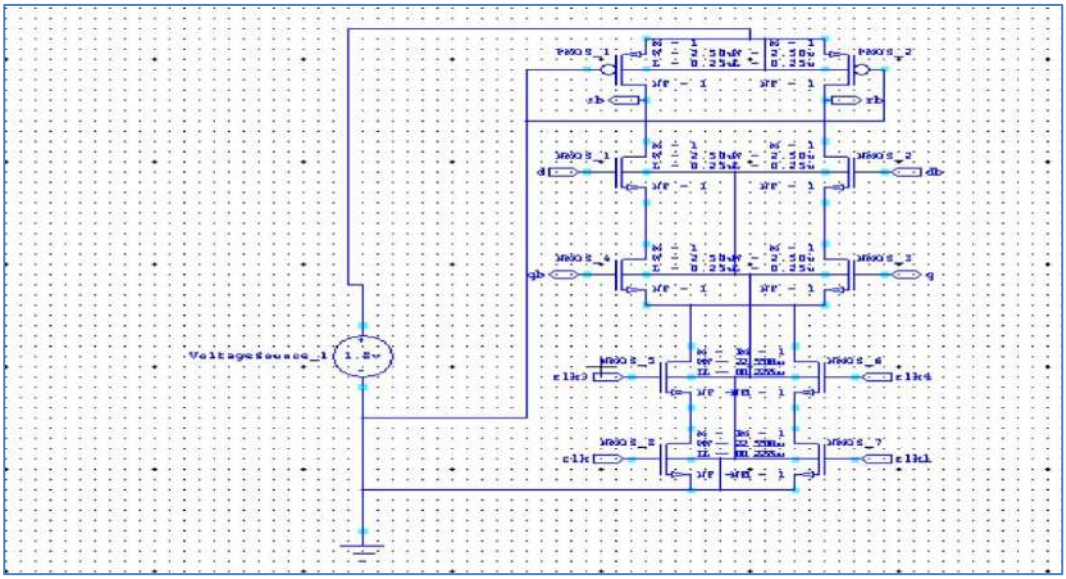


(b). Static latch

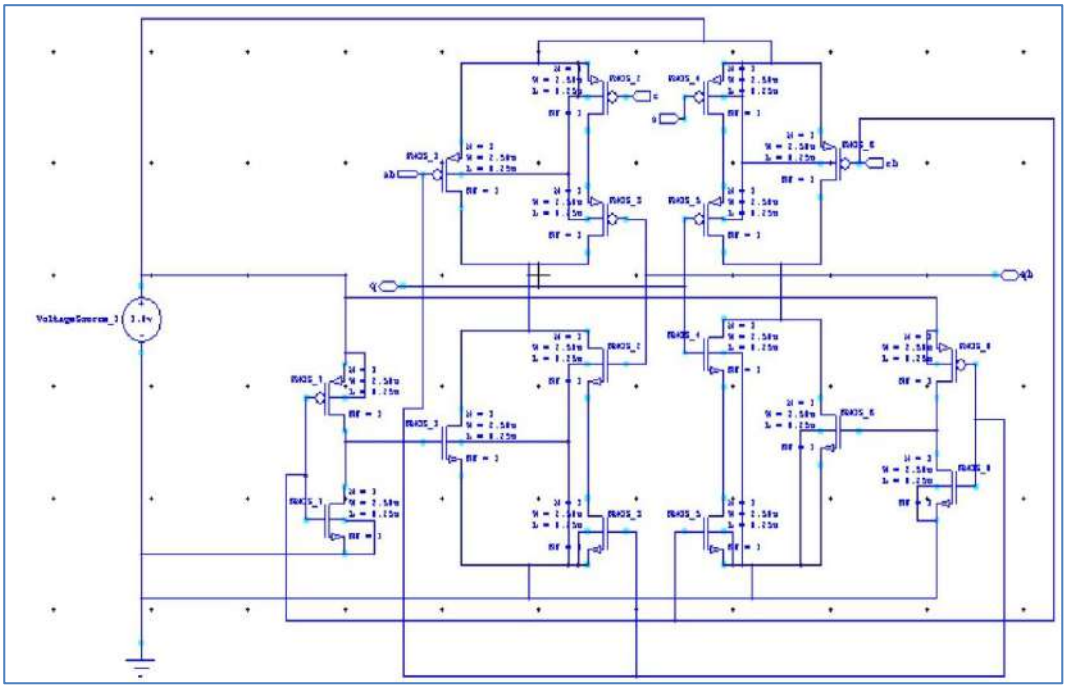
Figure 3.11 Static output-controlled discharge flip-flop (SCDFF)



(a). Adaptive clocking inverter chain



(b). Front end sensing stage



(c). Nikolic's latch.

Figure 3.12 Adaptive clocking dual edge-triggered sense amplifier flip-flop

The PMOS transistor P2 serves as the trigger node in the inverter queue whereas the CLK is small in the CLK4 production. The transistor N3 is switched off when the CLK3 is down. This is done in such a way that the CLK signal is not affected by it. We break down the inverter loop CLK3 and CLK4 to prevent the front-end sample information without including the up and down surface of the CLK section. If this system is not used, the CLK3 and CLK4 will be elevated.

3.3 SUMMARY

This chapter presents various exiting Flip Flop designs used for various VLSI applications. Some of the designs are used for low power applications. From the above discussion, it is identified that, each circuit performs according to their application. Based on the application requirement the performance of the FF are designed. The next chapter discuss about the proposed Flip Flop designs particularly designed for low power, high speed applications in recent days.

CHAPTER 4

PROPOSED FLIP FLOP DESIGNS

4.1 OBJECTIVES

The Modified Clock Gated Dual-Edge Triggered–Sense Amplifier (MCGDET-SA) Flip-Flop (FF) is proposed to enhance efficiency through the reduction of energy usage. This is achieved by lowering the energy required to change the clock which reduces the interval and prevents the energy leakage. Contrary to several previous gated FFs, MCGDET-SA FF includes holding properties to reduce consumption and alter the methods of switching circuits from inactive to active and passive to inactive. The energy dissipation is achieved by improving the response route. Fewer transistors are used to decrease the region of silicon in the current gating technique. The suggested Sense Verstarker FF reduces the time and improves the velocity at which the energy usage decreases further. This research directed at combining all of the above-mentioned functions with an altered clock gated enhanced flip-flop for small and high efficiency VLSI applications. The suggested FF is modelled and the outcomes are checked for different feed voltages. The test outcome demonstrates improved power usage and delayed results compared to the other FF frameworks.

4.2 PROPOSED APPROACH

In this research work, it is studied comprehensively about the various existing FF architectures, analyzed the limitations and planned a new Modified Clock Gated Sense Amplifier (MCG-SA) based FF circuit based on the compelling advantages, speed in operation, less area utilization and low

power consumption. The proposed MCGDET-SAFF circuit is designed and simulated by different methods within digital channels like DSP and Microprocessor. The first MCG-SAFF is used to obtain a considerable power reduction by integrating DET mechanism and conditional pre-charging. Also, by exhausting haste symmetrical latch, the MCGDET-SAFF is capable to accomplish lower power dissipation and delay. The proposed design has considered the baseline circuit, which is upgraded to develop a novel CGFF which decreases the power dissipation further. Also at low switching activity, the second proposed FF design gives more power saving additionally.

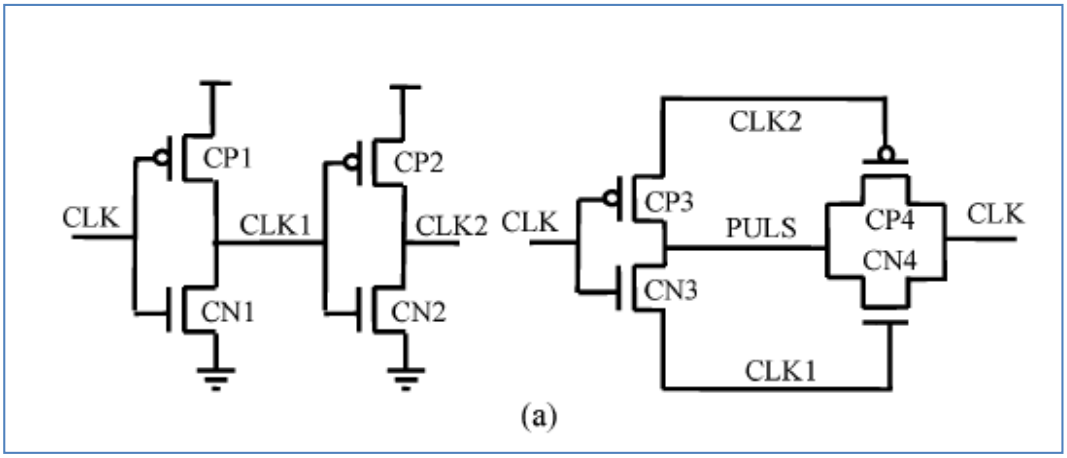
The integration of average delay and power is energy consumption. Power is directly proportional to the square of the voltage. One of the ways to obtain power consumption is by reducing the voltage usage. It also helps to diminish the logic speed. In various digital filters under DSP it is necessary to preserve the computation and throughput at a determined threshold. To maintain the performance parallel architectures are used as a low-level voltage supply. DET Flip-Flop devices are used to realize these concepts. Also, to reduce the delay, sense amplifier FF is integrated. But new VLSI circuit system demands low power for high-performance applications. Hence this research work motivated to design a novel modified clock gated dual edge triggered sense amplifier Flip-Flop for reducing the power utilization, power dissipation, delay thereby to increase the performance of the system which is used for any low power and high-performance applications.

4.3 DUAL-EDGE TRIGGERED SENSE-AMPLIFIER FLIP-FLOP (DET-SAFF)

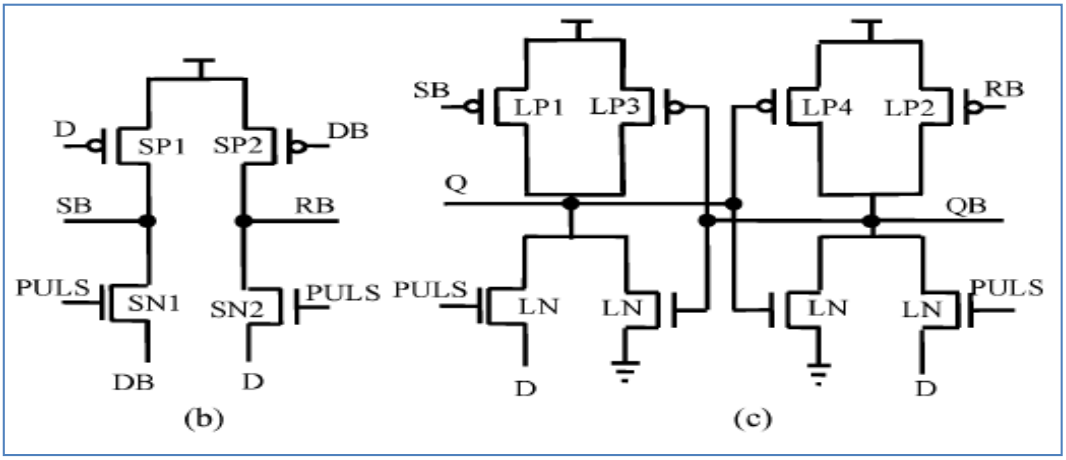
Figure 4.1 shows the schematic representation of DET-SAFF. The pulse generator is shown in Figure 4.1 (a) which generates a pulse signal. Mutually, all flip-flops in the circuits can share the pulse generator when they

are located nearby. Basically, in sense amplifier, if D is low SB will be high and vice versa. Figure 4.2 (b) and (c) shows the sensing and latching stage of the DET-SAFF. The conditional pre-charging technique is applied here to eliminate the repeated transitions in the central interior nodes. SP1and SP2 is the input controlled PMOS transistors, which is implanted in the pre-charge paths of nodes SB and RB. If D is set up as high for n cycles, then the SB will discharge in the first cycle only. SB is floating when the PULS are low and when PULS is high, it came to the flat state DB for the subsequent periods. But in the case of RB, it is required to pre-charge at the first cycle, and in the remaining sequences, it will be in the high state. Due to this charging activity, the significant path of SB and RB is simplified, and it contains only one signal transistor. By default, it reduces the discharging time considerably. Finally, this sensing stage becomes low-power and high-speed features.

Meanwhile, to pull up transistor by turning on and charges the output node Q to a high state by setting up the node SB as low. To pull-up, the output nodes, a high-speed symmetric latch is introduced to make use of SB and RB. The pull-down path is modified further. It includes PULS controlled NMOS pass transistor, during which D (DB) straight forwardly fed to the Q(QB) node. It is to increase the speed from low to high output since the high-speed symmetric latch circuit instantly captures the input signal once the PULS generated. Here the low-to-high latency will also be enhanced.



(a) – Dual Pulse Generator



(b) Sensing Stage **(c) Symmetric Latch**

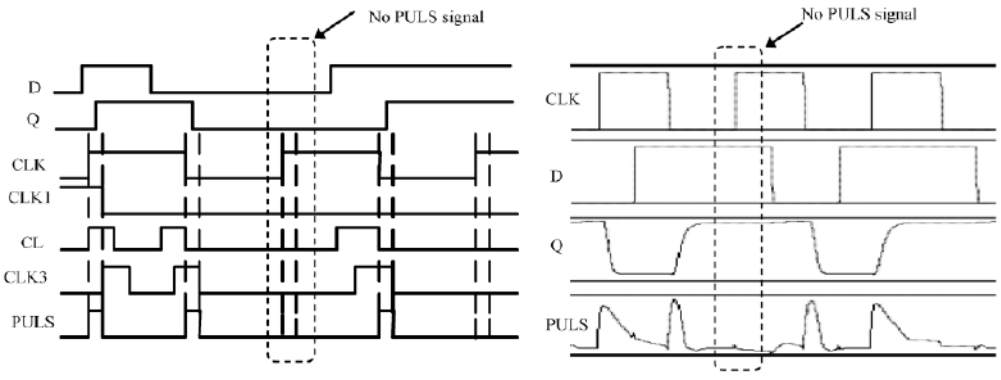
Figure 4.1 Dual Edge triggered Sense Amplifier Flip-Flop

The output node will not be charged only by pull-up transistors (LP1 & LP2) and also accused by the pass transistors (LN1 & LN2). Pass transistors may not load fully, but it can help with the pull-up transistors. LP3, LP4, LN3, and LN4 are the minimum size internal transistors designed for the point of maintaining the output state when the Flip-Flop is stable. In the proposed method the power reduction methods are only applicable for the latch part of the Flip-Flops. The pulse generator for all time is operating even when the input invokes no output changes for the switching activity of the clock signal is 1. This unwanted transition makes the power to be wasted particularly for low power applications. Conditional pre-charging is applied

here to avoid this power wastage. The main benefit of DET-SAFF is high speed and low power. But the redundant transitions, particularly at low switching activities, lead a lot of energy to be wasted.

4.4 CLOCK-GATED SENSE-AMPLIFIER FLIP-FLOP (CG-SAFF)

To eliminate the unnecessary transitions in the pulse generator, CG-SAFF is introduced. It used the DET-SAFF circuit as the base circuit and integrates it with the clock gating technique. This technique is mainly utilized to diminish the active power indulgence in synchronous circuits. This circuit called a digital circuit, and a clock signal synchronizes the components of it. Here the clock gating considered an event. The timing diagram and simulated waveform are shown in Figure 4.2 (a) and (b) respectively. The schematic diagrams of CG-SAFF, sensing stage, and latching stage are shown in Figure 4.3 (a), (b) and (c) respectively.

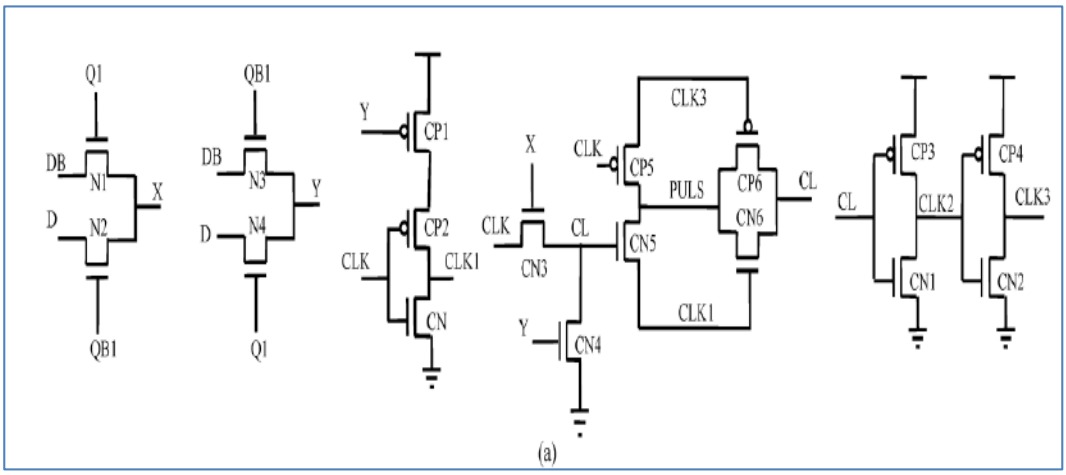


(a) (b)

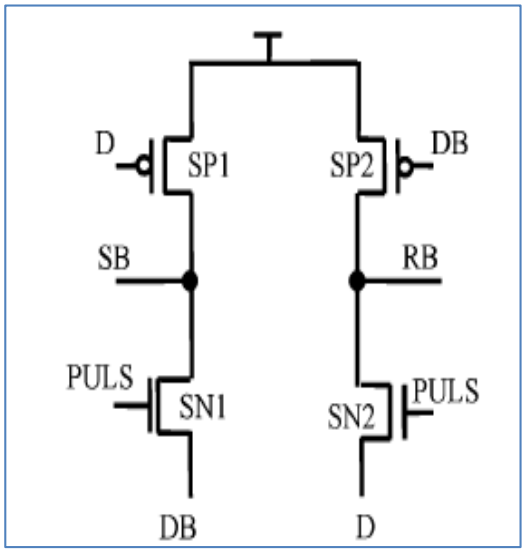
Figure 4.2 (a) CG-SAFF Timing Diagram (b) CG-SAFF Simulated Waveform

In this design, two comparators are used to match up to the prior and present input values. Also, it is used to produce X, Y signals using

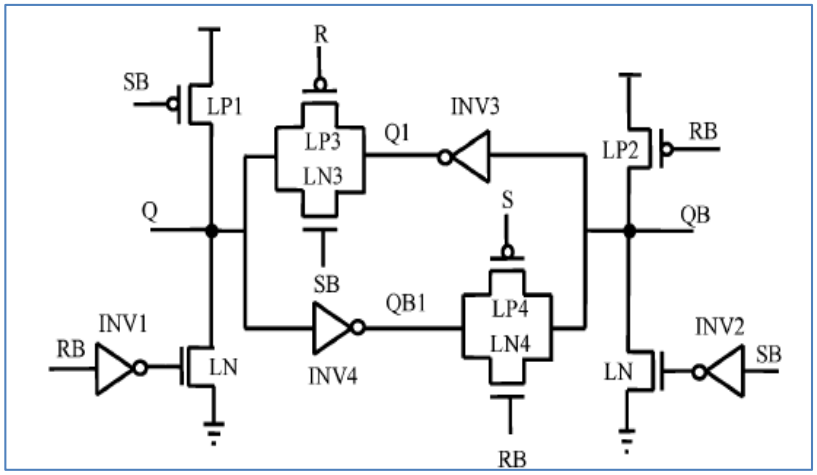
different inputs D and DB and to the outputs Q1, QB1 which is used as power signals. If D is found as varied in Q1 of Q, then X is set up as high and Y is set up as low. At the same time, the transistor N3 turned on for allowing the clock signal to go through as CL (Gated clock). Also, P1 is set to ON to force the CLK1 signal to high before getting more upper edge of the clock. Hence to pull-up, the PULS signal to high, transistor N5 and the transmission gate are Switched ON. When the CLK1 is down to low, then the transparent window blocked after a specific stage, and CLK3 is pulled up.



(a) Schematic Diagram



(b) Sensing Stage



(c) Latching Stage

Figure 4.3 Clock Gated Sense Amplifier Flip-Flop

Likewise, a short transparent period was created at the rising edge of the clock. Here CLK1 is used for pulse generation and not CLK2. It is to ensured that race problems are prevented and the flip-flop gets the data only at the triggering boundary of the clock. CL is little and CLK3 elevated at the falling edge. While the CLK3 is low, the sampling window will be closed simultaneously. D remains in the same state for successive clock cycles and same as that X is small and Y is high. At low switching activity, CL has been forced down; as a result, the flip-flop takes the advantage of power dissipation, and at the same time, the area of the design is considerably more. The sensing stage is similar to the DET-SAFF and it has modified Nikolic's latch to hold buffered and differential outputs. The output Q1 and QB1 as an alternative of Q and QB are used in pulse generator to get the PULS signal. This CG-SAFF has the advantage to low switching activity.

4.5 MODIFIED CLOCK GATED SENSE AMPLIFIER FLIP-FLOP (MCG-SAFF)

The working principle of the MCG-SAFF is same as that of CG-SAFF. Also with the principle of CG-SAFF, MCG-SAFF includes the additional circuit in X to avoid asynchronous data sampling.

In CG-SGFF, for the input transitions on D, asynchronous pulse generation may occur on the internal clock during global clock CLK=0. In a small period, node X will be going from charge to discharge before the switch turns off.

The asynchronous transition happens at the output if the value of X is powerful enough to flip the nodes to the production. If it does not happens and also the first activate of the inferior pathway has not efficiently conceded the input D to the output, then the higher path serves as a support that will trigger at the subsequent falling edge of internal clock C.

There are various sets of transistor sizing that can cause the asynchronous data sampling to fully appear, partially appear or may hide while adjusting the transistor sizes around Node X. The circumstance that creates the asynchronous transition occurs when the voltage of Node X attains the critical value to Flip-Flop the output.

The circuit's parameters such as transistor size are personalized to remove Asynchronous Data Sampling which is shown in Figure 4.4.

1. Balanced size
2. Modified I
3. Modified II

4.6 METHOD TO AVOID ASYNCHRONOUS DATA SAMPLING

In this method the CLK is restricted by the evaluation of D and Q. If D has distorted because of the final clock move and is dissimilar from Q, then CLK will go to the second comparator to match up with the C. This CLK and C comparator reins the switch T2 between the CLK and C.

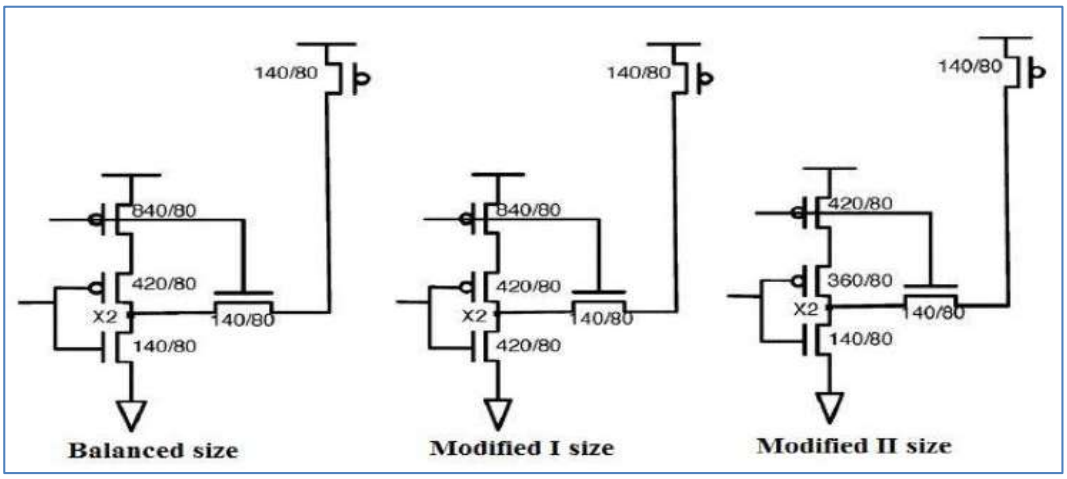


Figure 4.4 Modified Circuits on X

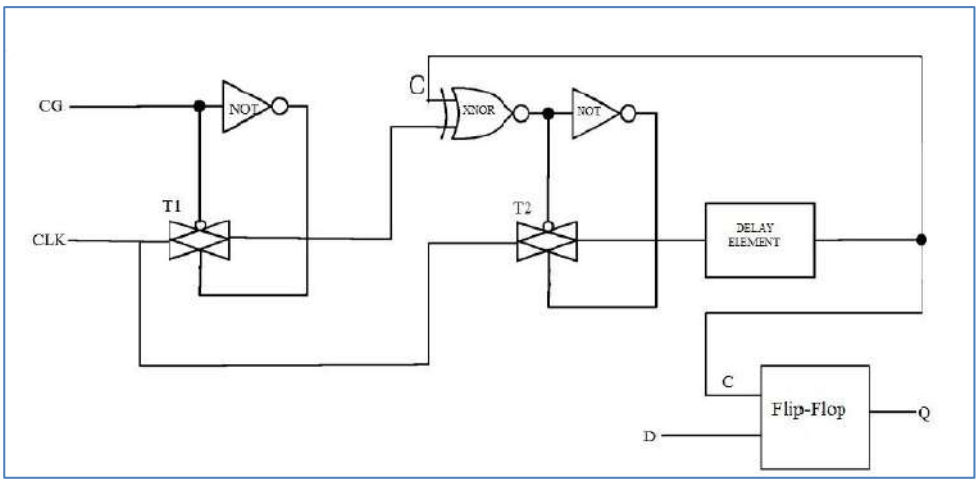
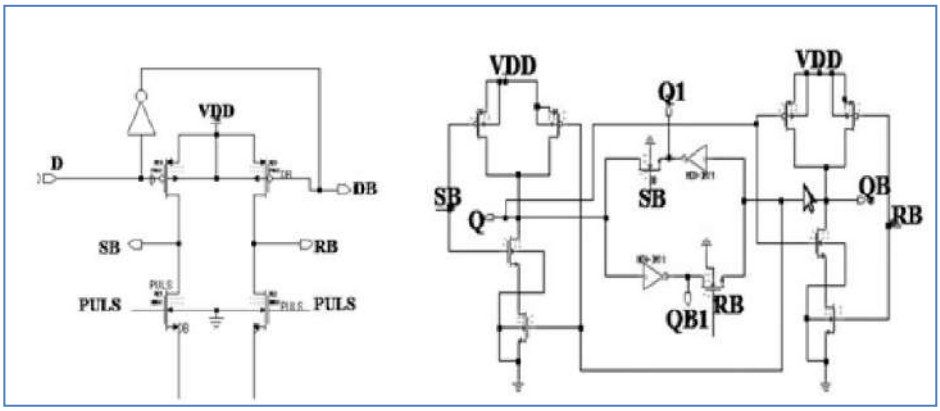


Figure 4.5 Method to avoid Asynchronous data sampling

At the moment of changing D, CLK differs from C there is an occurring of Asynchronous sampling. Though with the second CLK and C comparator in Figure 4.5, the knob T2 will stay OFF when CLK ≠ C and C match with CLK. In the succeeding half cycle, the knob T2 turns ON, where CLK = C, but because they are equal, the Flip-Flop will not trigger until C changes, which follows CLK when is ON. Here, the modified II circuit gives the better power consumption when compared to another adjusted size.

4.7 MODIFIED CLOCK GATED – DUAL EDGE TRIGGERED SENSE AMPLIFIER FLIP-FLOPS

The proposed Sense Amplifier Flip-Flops include three stages named the pulse generating stage, sensing stage and the latching stage. The first two stages are similar to the Dual Edge triggered Sense Amplifier Flip-Flop (DET-SAFF) which is shown in Figure 4.1. The proposed MCG-DET SAFF is shown in Figure 4.6. Based upon Sense-Amplifier Flip-Flop (SAFF), the pulse generator samples the dataset. In the CLK rising edge, CLK and CLK3 together are high for a small duration of time and CL and CLK4 in the CLK falling edge.



(a) Sensing Stage (b) Latching Stage

Figure 4.6 Proposed Modified Clock Gated – Dual Edge Triggered Sense Amplifier Flip-Flops

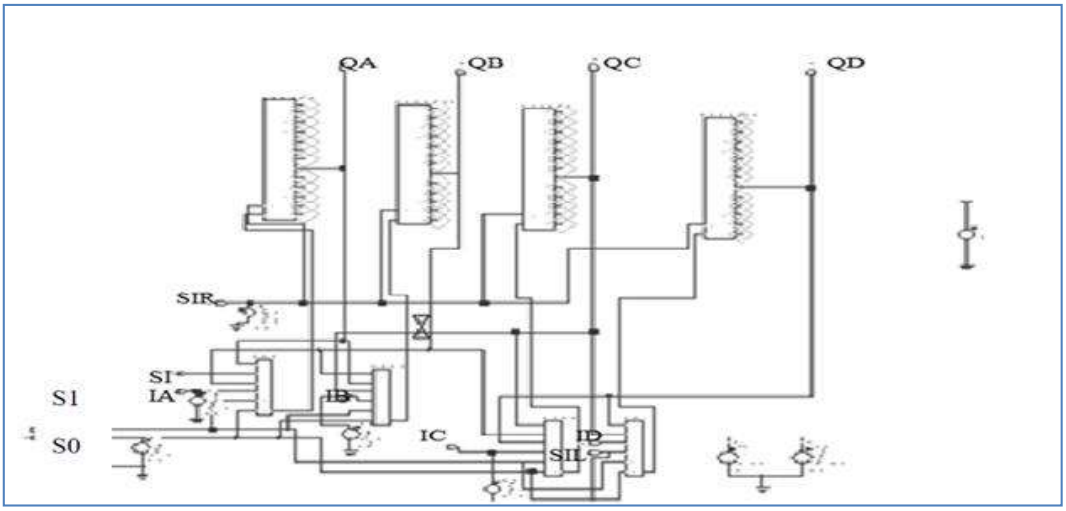


Figure 4.7 Universal Shift Register

To pull-up the output nodes, a high-speed symmetric latch is introduced to make use of SB and RB. RB is put in a high state if the input of D is high and at the same time transistors involved is in the state of pull-down network. It will make the quick discharge path recognized from QB to Ground. And if D is low, SB will set too high. Meanwhile, to pull up transistor by turning on and charges the output node Q to a high state by setting up the node SB as low. The internal set up is modified to get buffered differential outputs Q1 and QB1. It is to increase the speed from low to high output since the high-speed symmetric latch circuit instantly captures the input signal once the Pulse generated.

In the proposed Flip-Flops, the new design introduce a universal shift register to hold up the previous state which is shown in Figure 4.7. If the input selected to the global shift register, S1=0, and S0=0 then the shift register holds the former state. If S1=0 and S0=1 then the entry performs shift right operation by taking a serial input, and in reverse, if S1= 1 and S0 = 0 then shift left activity will be performed. And at last if for the input S1=1 and S0=1 parallel input and parallel output operation will be performed.

4.8 SUMMARY

This chapter discussed about various Flip Flop designs and a novel Flip Flop design architecture for low power, high speed applications is implemented. From the above discussion, it has been decided that a clock gated dual edge triggered sense amplified Flip Flop can be modified for improving the efficiency in terms of low power consumption and speed process. It can be identified by investigating the main features of various Flip Flop designs and integrated into modified clock gated dual edge triggered Flip Flop, which can perform well than the other designs.

CHAPTER 5

EXPERIMENTAL RESULTS AND DISCUSSION

5.1 OBJECTIVES

This chapter presents all the experimental/simulation results obtained from various architectures of Flip Flop. The findings highly recognize the efficiency of the suggested dual-bound, altered clock-bound, enhanced Flip Flop sensor for small energy and high-speed applications

5.2 RESULTS FOR DUAL EDGE TRIGGERED FLIP-FLOP

Initially in the first stage, the dual edge triggered Flip Flop design circuit is simulated and the results are verified. In this stage, DETFFs (1 and 2) were suggested as better designs and designed with CMOS technology of GPDK 90nm and programmed with SPECTERE simulation tool. Adhering the effect of RC in the layout, Programming and simulation were done with variable supply voltages and clock frequencies keeping data pattern fixed. The results of the simulation were compared and presented below which shows the differences in set up time and hold time of various DETFFs.

The results obtained from conventional DETFF is compared with the results obtained from DETFF-1 and DETFF-2 in terms of tpd delay, power consumption, PDP,t_{su}, t_{hl}based on the clock frequency and power supply. From the Table 5.1, it is noticed that the 2-DETFF performs well than the others. Also, various parameters of the waveform were taken and shown in Figure 5.1. In accordance to the parameters given in Table 5.1, the waveforms are taken from the experiment and it is given in Figure 5.1. From the

waveform, it is identified that in accordance to the increasing D-clock delay (ps), the Clock-Q-delay (ps) is decreasing and becomes stable. The traditional DETFF, in spite of its less propagation delay, higher power consumption due to the fabrication of many transistors for its working, is to be considered seriously. The recommended 2-DETFF shown above has no MOS (latch) in the output end as fabricated in traditional devices. But the recommended 1-DETFF eradicates the demerits of above said DETFFs in the both power and time delay sector as it is formulated with lower chip area as compared to the previous ones.

Table 5.1 Comparison of DETFFS Parameters

S. NO	Circuit used	Clock freq (MHz)	Power supply (V)	Tpd delay (ps)	Power (µW)	PDP	Tsu (ps)	Thl (ps)
1	Conventional DETFF	500	1.2	85.45	15.7	1.34	-2	150
		500	1.5	66.46	26.23	1.74		
		500	2	52.78	54.54	2.87		
2	Proposed -1 DETFF	500	1.2	76.52	16.84	1.34	20	75
		500	1.5	53.61	28.7	1.53		
		500	2	47.64	61.29	2.91		
3	Proposed-2 DETFF	500	1.2	61.93	15.46	0.95	15	50
		500	1.5	48.17	26	1.27		
		500	2	34.62	54.32	1.87		

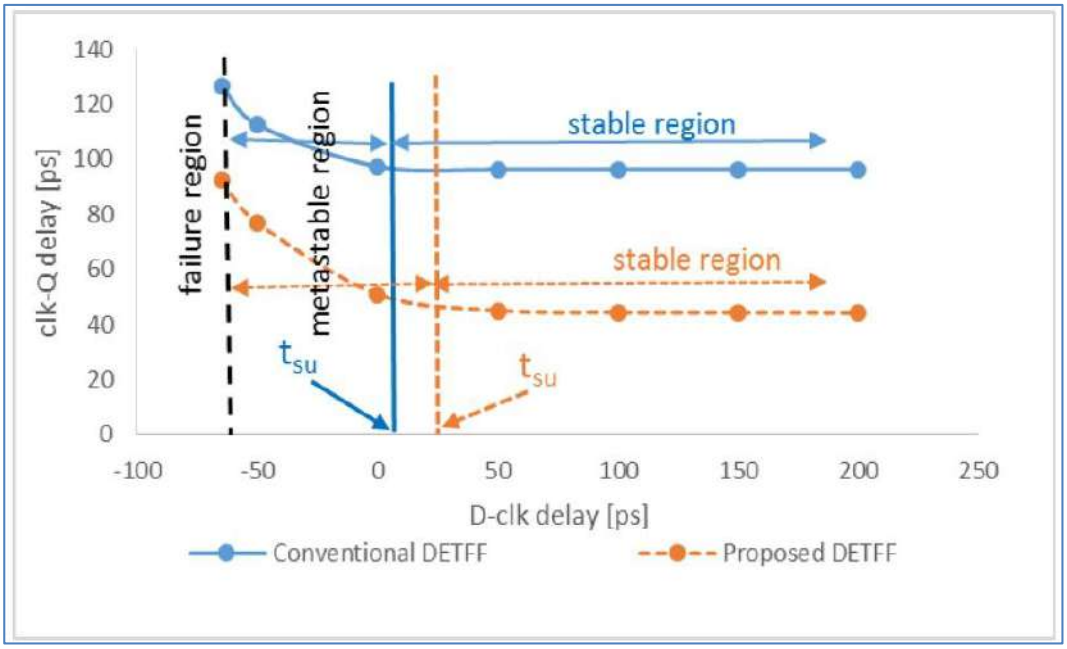


Figure 5.1 Metastable, stable and failure zone

The delay occurs between clock latching edge and the edges of Q are termed as propagation delay. Four types of states can be illustrated between Q and clock. The Q can rise and fall in the falling edge of the clock pulse and Q can rise and fall in the rising edge of the clock. With the average of all the delays in four predicted states, were taken as the overall propagation delay. Similar to the above comparison, the power supply and the power consumption ratio is calculated for all the three types of DETFFs, and the obtained results is given in Figure 5.2.

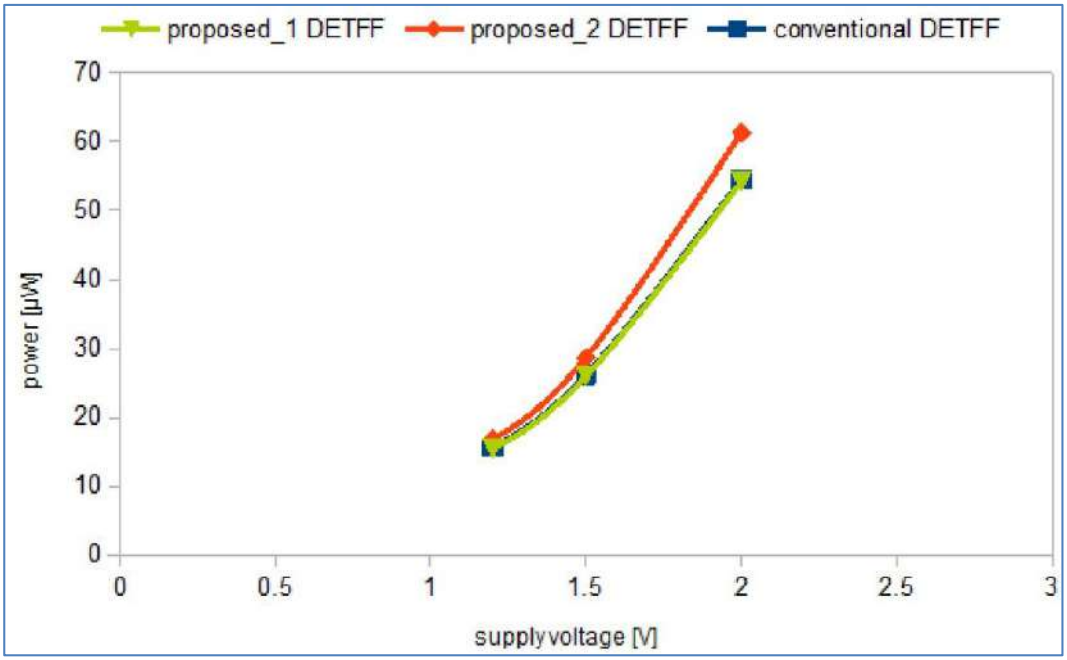


Figure 5.2 Power vs Supply Voltage curve

From the obtained results, it is identified that for a fixed supply to a range of voltage supply, the power consumption is increased. For example, after the voltage supply becomes 1V, an amount of power is consumed for processing. Comparing with all the DETFF designs, the proposed 1-DETFF design consumed less power than the other two DETFF designs such as conventional DETFF and 2-DETFF.

Similarly, the delay is calculated in accordance to the supply voltage. From the Figure 5.3, it is noticed that for all the three types of DETFF designs the delay is decreased for increasing supply voltage. Comparing with one another, the delay taken by 1-DETFF is very less than the other two designs.

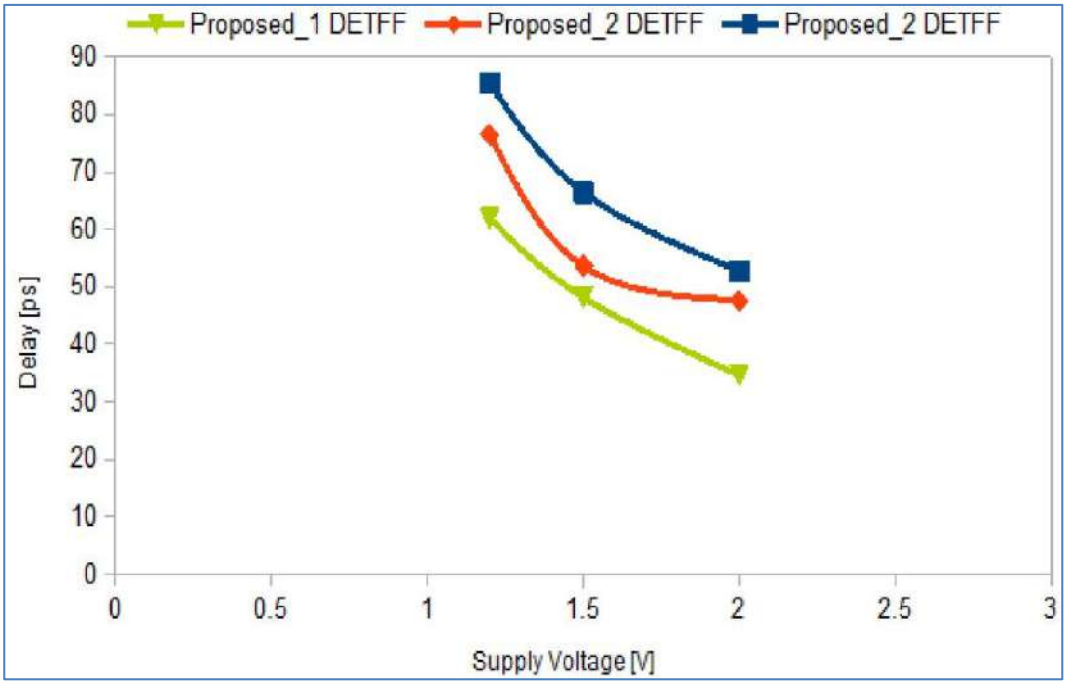


Figure 5.3 Delay vs Supply Voltage

5.3 RESULTS OBTAINED FROM CPS-FF

Second, various logic methods the CPS-FF is carried out and the performance is proved. From the results that it had obtained the best performance values regarding reduced delay, power and area. The advantages of an effective circuit system are simple gates, no swing restoration circuitry and single-rail logic property. In the existing system-1 it has been summarized that various approaches are used for reducing the power consumption of the clocking methods. CPS-FF initially decreases LSDCC-FF energy usage by removing unwanted inner information holding the node switch. Therefore less swing clock reverse Flip- Flop reduces clock channel power usage by reducing the clock's frequency swing. Moreover, the capability of the clock integrated circuits in CPS-FF is also reduced. Finally, the proposed CPS-FF utilizes a dual edge trigged operation and a low swing for reducing the power consumptions in the clock network. So, the CPS-FF has not involved redundant data which holds the switching. From the experimental result the

number of transistors, clocked transistors, power consumption and power dissipation are compared with one another and the comparison result is given in Table 5.2. The bar chart of Power Consumption Comparison is shown in Figure 5.4.

Table 5.2 Performance Comparison

S.NO	Methods	No of Transistors	No of clocked transistors	Power(µW)	Power Dissipation
1	LSDFF	28	3	132	26.3
2	CPSFF	22	2	116	19.4
3	CPS FF with pass transistor Logic	18	2	110	14.2

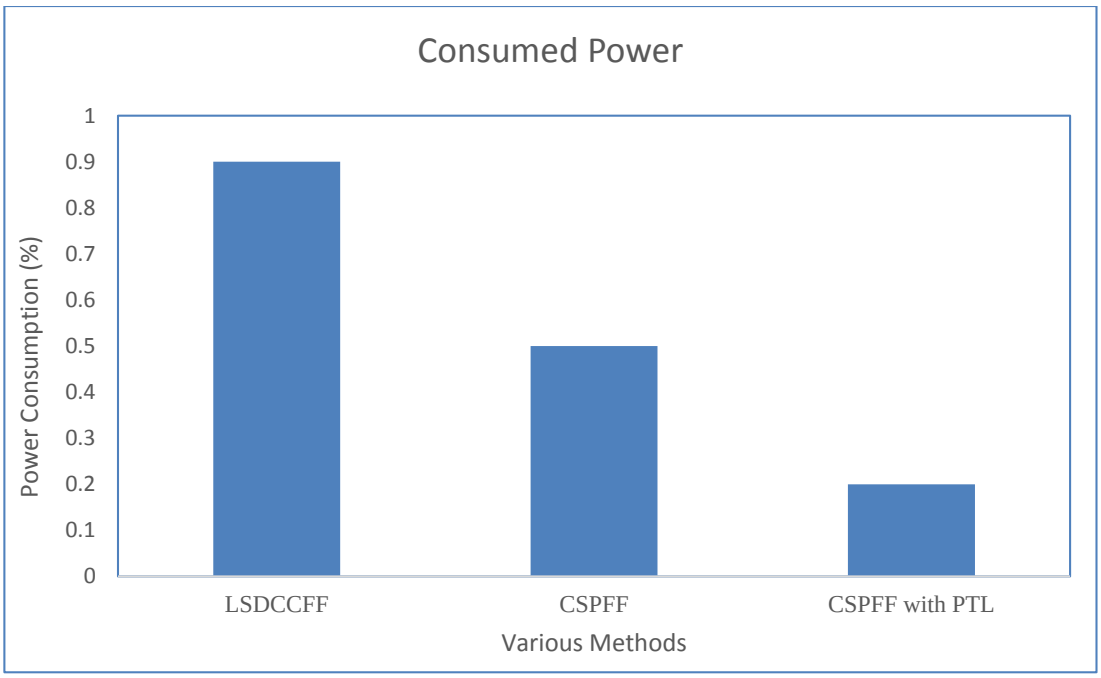


Figure 5.4 Power Consumption Comparison

The Simulation output of LSDCCFF, is shown in Figure 5.5

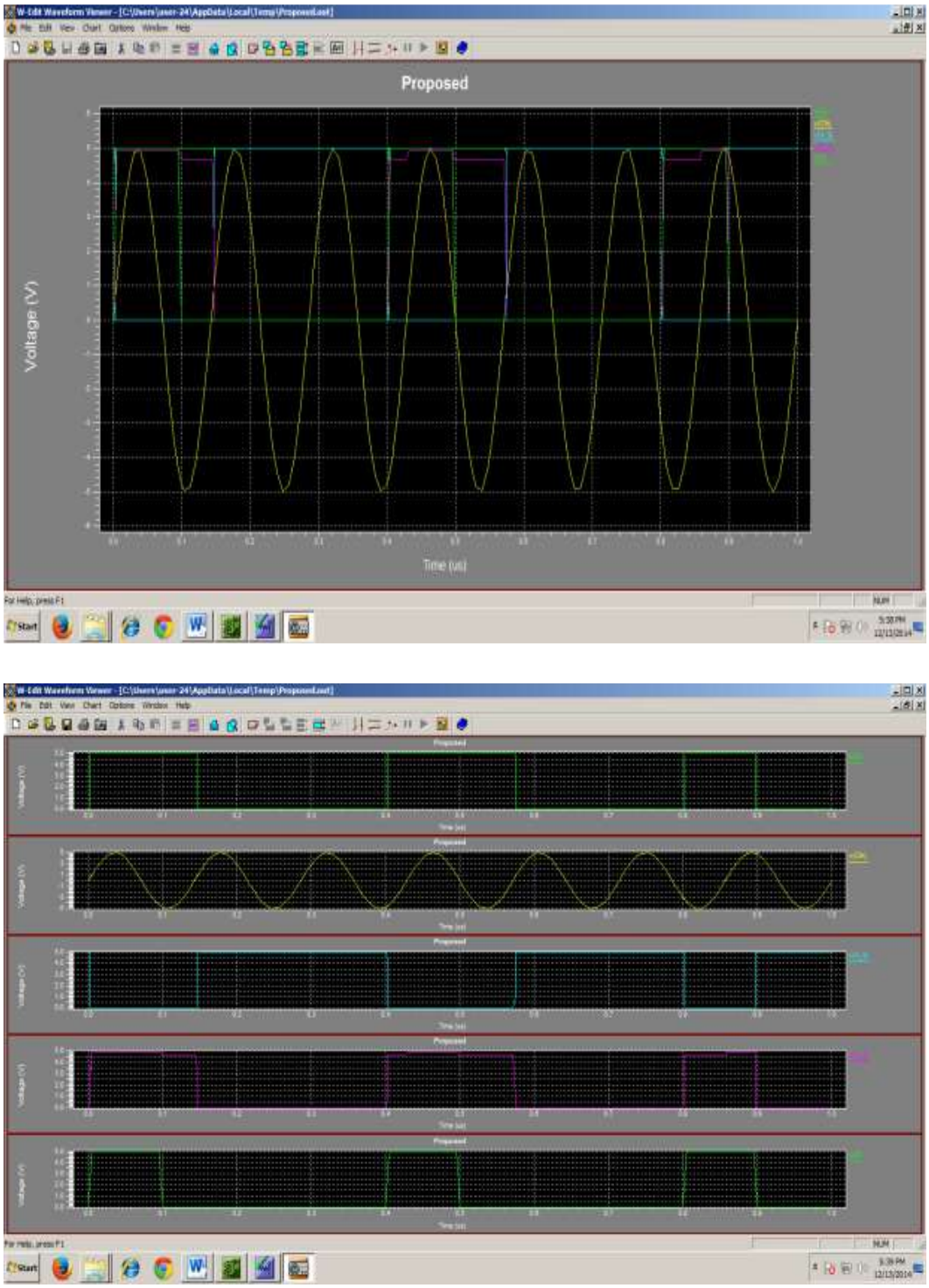


Figure 5.5 Simulation Output of LS-DCCFF

The Simulation output of CPSFF with Pass Transistor Logic is shown in Figure 5.6.

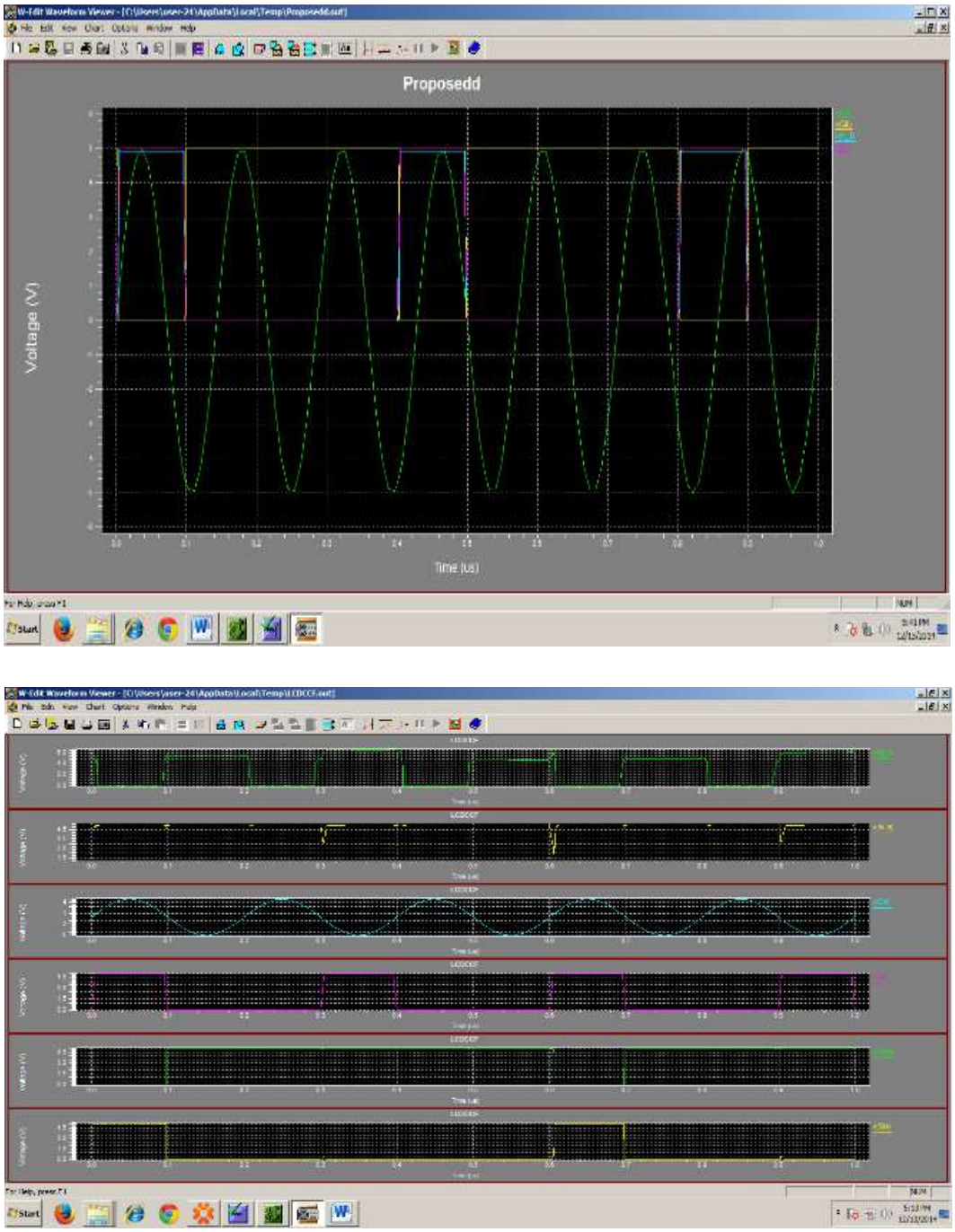


Figure 5.6 Simulation Output of proposed method (CPSFF)

The Simulation output of CPS with Pass Transistor Logic is shown in Figure 5.7.

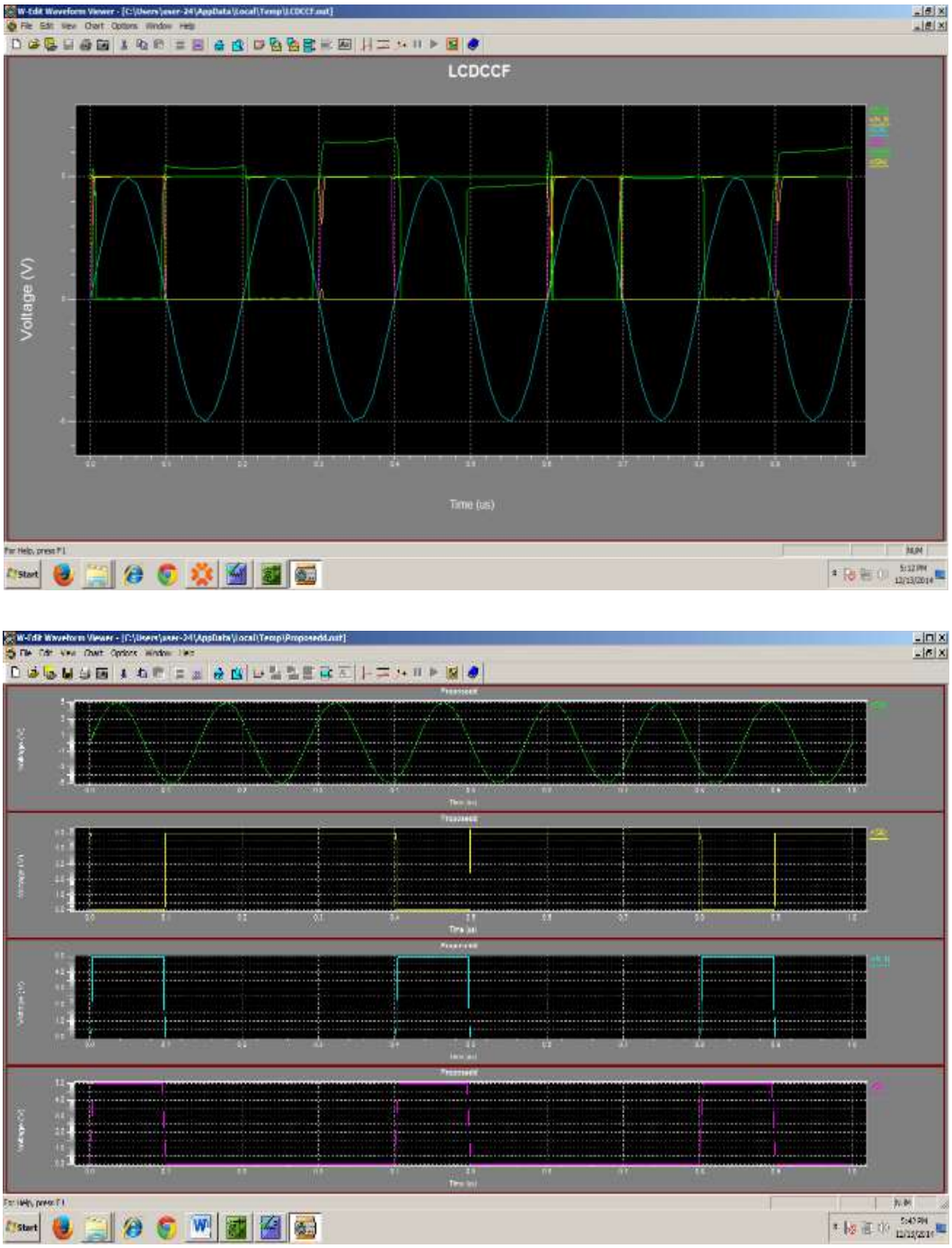


Figure 5.7 Simulation Output of CPSFF with Pass Transistor Logic

From the results and discussion, it is analyzed that various traditional Flip Flop methods and it has been understanding the new methodology for creating a novel FF design in 0.18μm CMOS process. All the FFs are optimized in terms of power consumption and delay. The low-swing voltage for LSDCCFF is 1V and the load capacitance of the output is assumed as 100μF. The output waveform obtained from the simulation-based experiment for two FFs is illustrated in Figure 5.5 and in Table 5.2. From the results it is clearly noticed that Figure 5.7 shows that the lowest power consumption is obtained by CPSFF-PTL without affecting the input pattern. But the LSDCCFF and CPSFF incur high power consumption than the other designs though the input is 1. Using the proposed CPSFF-PTL, the average input switching activity of 0.3, the power consumption is highly reduced by 25.6%-44.6% than the conventional FFs.

5.4 RESULTS FOR VARIOUS TYPES OF DUAL EDGE FLIP FLOPS

Simulation findings for all Flip-Flops are achieved using T-SPICE at a 0.18μm CMOS technology using 1.8 V storage voltage. The simulations of the continuous simulated double-edge Flip Flop are shown in Figure 5.8. In Figure 5.8, DSPFF has a median capacity of 1.0079μw.

Dual-edge simulations of continuous pulsated flip flops are displayed as Flip Flop type D in Figure 5.8. This is the same as a postponed wave for the entry of information. The frequency of clocking is larger than the frequency of input, so the changes in the input have been deferred to check the result. DSPFF is averaged 1.0079μw in strength and is decreased to 0.757μw by lowering the power supply of threshold.

Figure 5.9 shows simulations of the SCDFF. SCDFF is 0.1536µw converting energy. It decreases up to 0.0357µw with multi-thresholding technology. The energy demand has been observed to be lower than before.

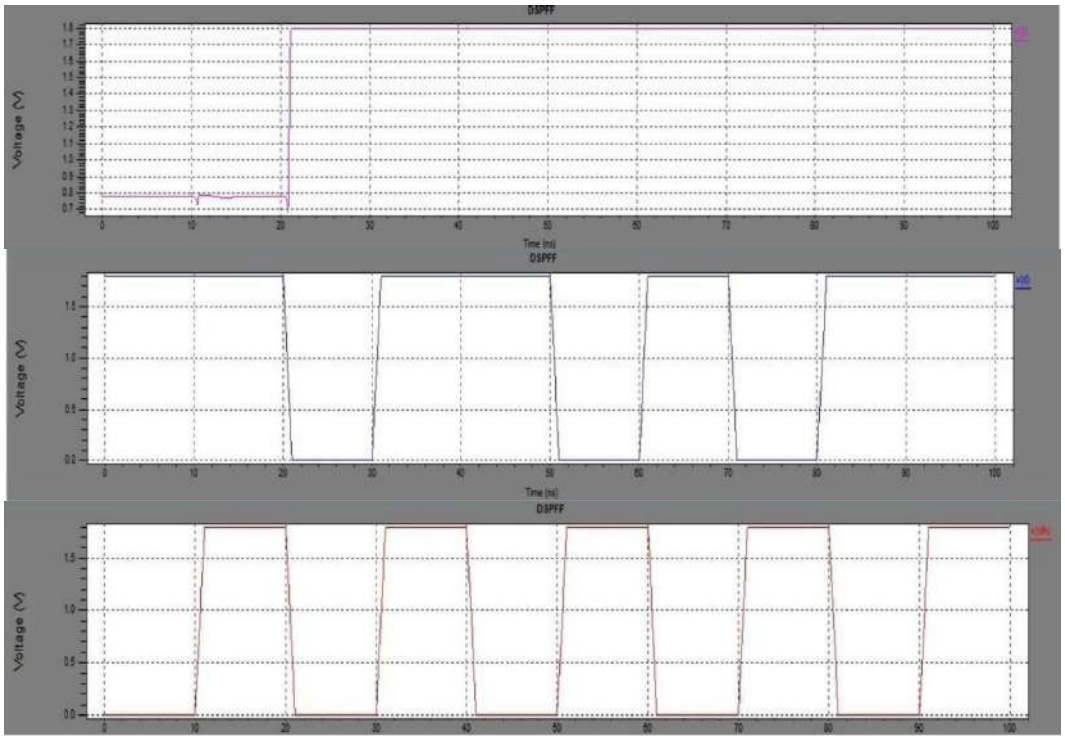


Figure 5.8 Simulations of dual-edge triggered static pulsed flip-flop

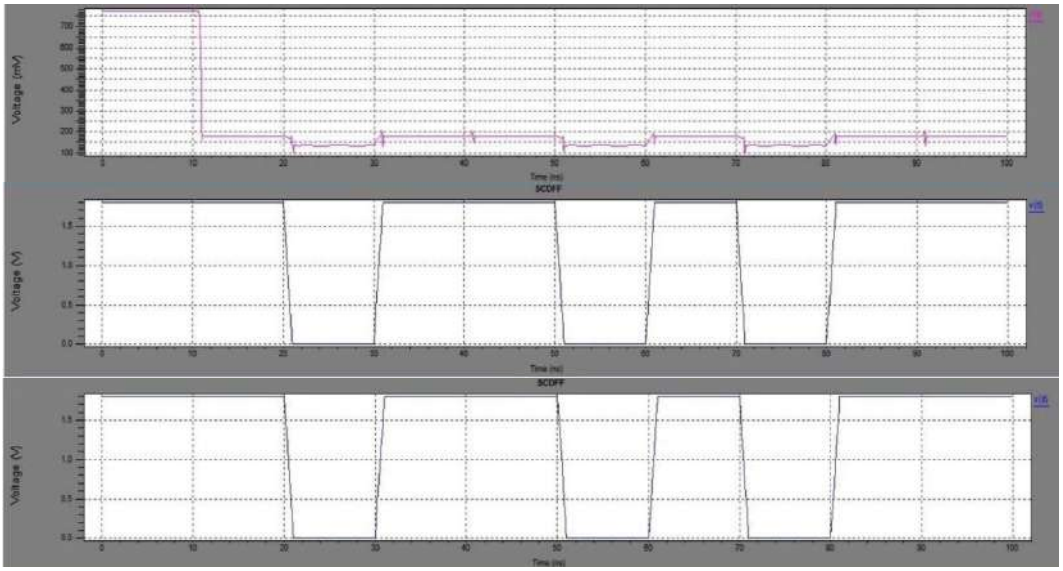


Figure 5.9 Simulations of SCDFF

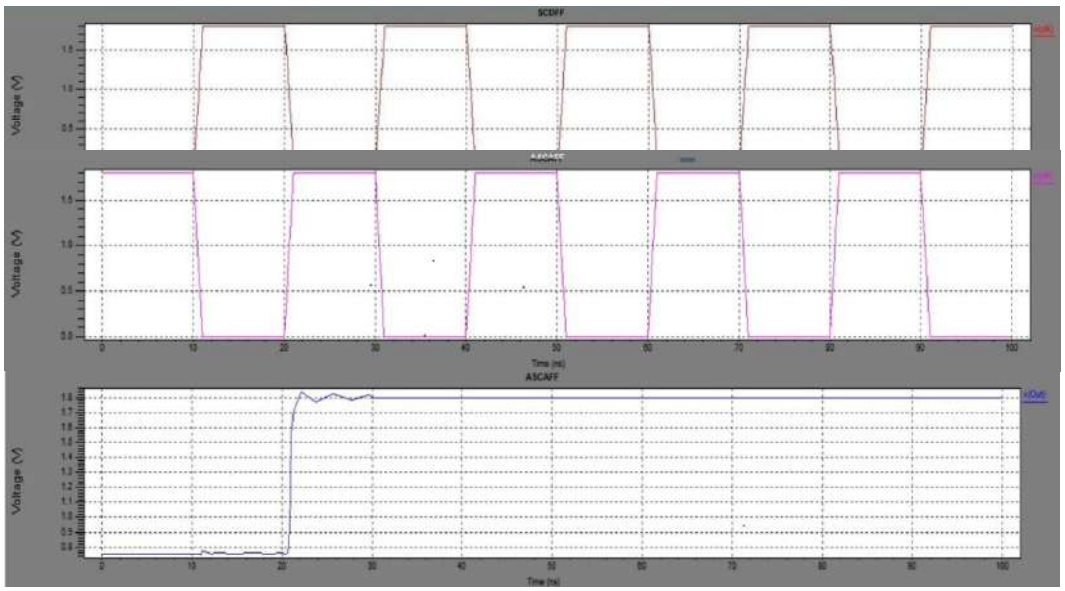


Figure 5.10 Simulations of adaptive clocking dual edge sense amplifier flip-flop (ACSAFF)

ACSAFF has 0.11472μw energy limit which is the ACSAFF conversion force. It is decreased to 0.050426μw by means of a multi-thresholding method and the obtained result is given in Figure 5.10.

5.5 RESULTS OBTAINED FROM PROPOSED DESIGN

The suggested MCGDET-SAFF was designed using the CMOS 0.13µm method technologies of national electronics Limited. The following Table 5.3 shows the set of all parameters used in the experimental setup and the experiment is carried out.

Table 5.3 Experimental setup parameter and its values

S.NO	PARAMETER	VALUE
1	CMOS	0.13µm
2	Operating Temperature	27 degree C
3	Supply Voltage	1.6 V
4	Tool	Mentor Graphics tool
5	Clock Frequency	0.8GHz
6	Load Capacitance	100fF

The obtained results of the proposed MCGDET-SAFF are verified regarding consumed power and delay. The performance of the MCGDET-SAFF evaluated by comparing the obtained results of various Flip-Flops offered in earlier research works. The complete performance analysis of the multiple Flip-Flops is given in Table 5.4 and Table 5.5. The bar chart of CLK-to-Q delay as a function of D-to-CLK delay and D-to-Q delay as a function of D-to-CLK delay is shown in Figure 5.11 and Figure 5.12.

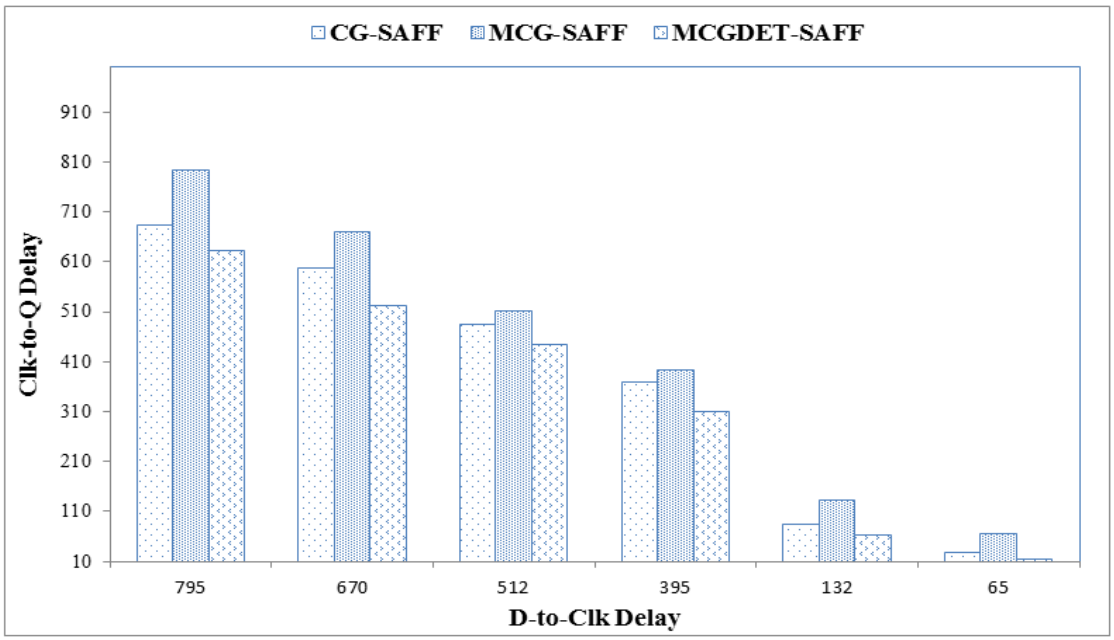


Figure 5.11 CLK-to-Q delay as a function of D-to-CLK delay

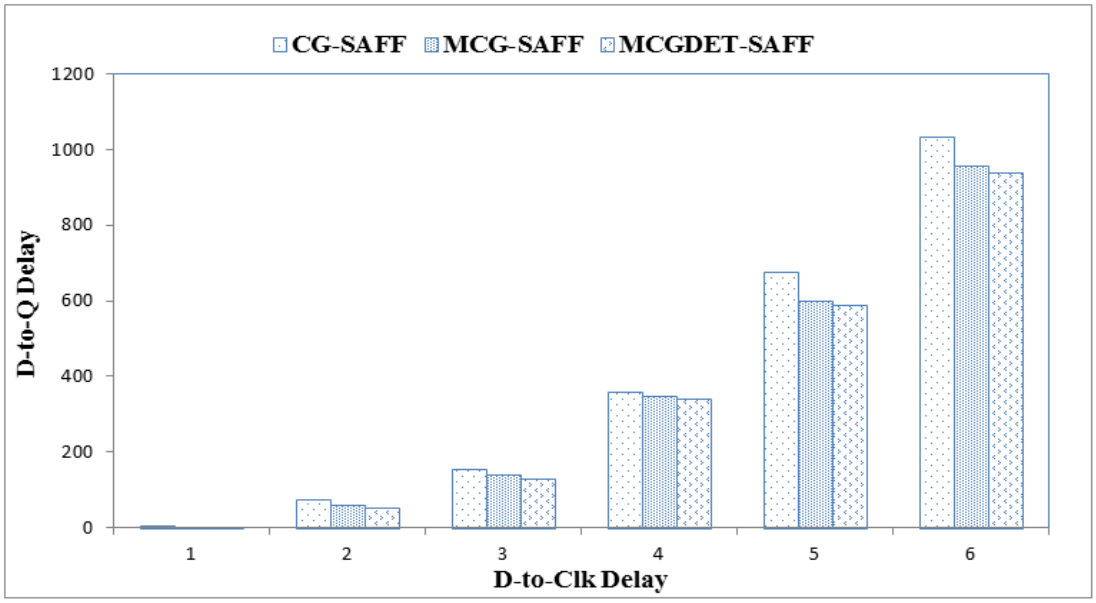


Figure 5.12 D-to-Q delay as a function of D-to-CLK delay

Table 5.3 Performance Analysis of CG-SAFF @1.8v at Different Operating Frequencies for Different Switching Activity

S.NO	Switching Activity	MOCF (GHz)	D-Q Delay (ps)	Clk-to-Q delay(ps)	Rise Time (ps)	Total Power Dissipation (nW)
1	25%	0.83	2646.88	642.01	1226.26	33.0154
		1	2547.87	542.91	1027.06	33.0154
		1.25	2050.97	445.96	829.15	33.0153
2	50%	0.83	2246.57	641.55	1225.66	33.0154
		1	2547.87	542.89	1027.16	33.0154
		1.25	2050.97	446.68	829.16	33.0154
3	75%	0.83	2646.97	642.01	126.26	33.0154
		1	2547.87	542.9	1027.16	33.0154
		1.25	2050.97	445.97	829.16	33.0154
5	100%	0.83	2246.57	641.57	1225.66	33.0154
		1	2547.87	542.9	1027.16	33.0154
		1.25	1653.97	448.08	829.85	33.0154

Table 5.4 Feature comparison of different FFs

FF Design	CG-SAFF	MCG-SAFF	MCGDET-SAFF
Layout Area (mm^2)	69.13	64.23	63.12
Min D-to-Q Delay (ps)	120.23	90.17	84.35
Average power (0% all-0) µW	10.25	12.07	7.55
Average power (0% all-1) µW	10.35	12.76	7.45
Average power (12.5% activity) µW	12.68	13.11	12.11
Average power (25% activity)µW	14.95	15.95	14.95
Average power (50% activity)µW	19.87	18.46	19.43
Average power (100% activity)µW	26.15	24.15	24.15
Optimal PDP (25% activity) pJ	4.08	1.58	1.58

From the results, it is obtained that the proposed MCGDET-SAFF has the lowest delay than the other FFs. It received 78% of the reduction in delay. Various test patterns can be used for simulating the FF designs. In this research work, six models are considered for multiple situations. The various probabilities are 25%, 50%, 75% and 100% for all 0's and 1's in data transition probabilities. The obtained results are given in Table 5.3.

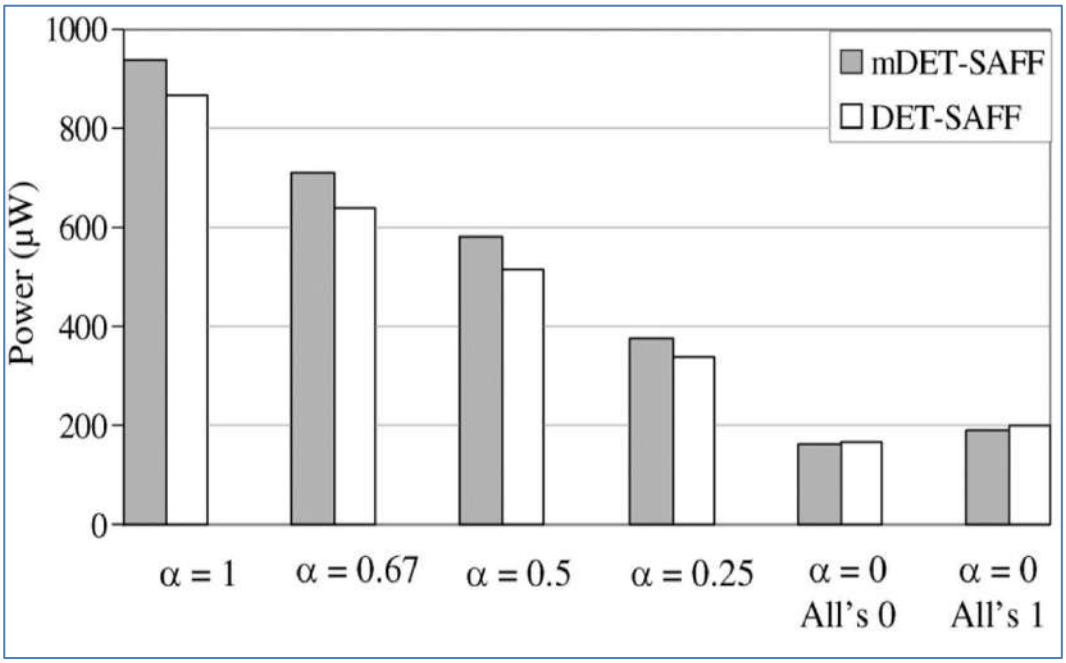


Figure 5.13 Comparison of Power consumption Among Modified and Proposed DET-SAFFs at different input

Figure 5.13 demonstrates the outcome of the energy dispersion evaluation at changing entry changing occurrences between both the DET-SAFF and the mDET-SAFF suggested. For PDP, the PDP of mDET-SAFF is 6.5% higher than the suggested DET-SAFF. The altered variant of the DET-SAFF suggested however has significantly enhanced CMRR compared to that of the DET-SAFF suggested. Furthermore, the suggested MCGDET-SAFF framework finished with the outcomes described in Table 5.4 as a stronger structure. The MCGDET-SAFF structure uses the lowest amount of technology associated

transistors; the design region is decreased. For instance, 10% of leakage energy reduction and approximately 20% increase the highest PDP in 25% of operation.

Table 5.5 Comparison Results of CG-SAFF and MCGDET-SAFF

Designs	MCG-SAFF	MCGDET-SAFF
Clk-to-Q delay(ps)	187.03	152.04
Min D-to-Q delay(ps)	592.03	307
Rise Time (ps)	79.809	90
Fall Time (ps)	800	199
MOCF (GHZ)	1.25	1.25
Number of Transistors	38	22

Table 5.6 Power Consumption Comparison

Name	Power Consumption using Conventional Methods	Reduced Power Consumption using Proposed Method
SCDFF	0.1536µw	0.0357 µw
DSPFF	1.0079 µw	0.757 µw
ACSAFF	0.11472 µw	0.050426 µw
MDETSAFF	-	0.049032 µw
MCGDET-SAFF	-	0.0432 µw

Table 5.5 shows the CG-SAFF and MCG-SAFF efficiency studies with MCGDET-SAFF. The MCGDET-SAFF suggested acquired the minimum Clk-to-Q interval between Flip Flops. It gained more than 80% of the backlog reduction. Eventually, the outcomes of the CG-SAFF, MCG-SAFF and MCGDET-SAFF reverse Flip Flops are given in Table 5.5. Furthermore, the suggested MCGDET-SAFF has achieved stronger outcomes from the laboratory outcomes, the energy dissipation for distinct entry switches activates for distinct FF models. With regard to PDP, the MCG-SAFF uses 6.5% more PDP than the MCGDET-SAFF. However, the proposed MCGDET-SAFF exceeds the other FF

models. In the last phase of the study project the suggested Flip Flop mentioned is likened to the suggested Flip Flop models in the earlier phases of the studies. The comparison output is given in Table 5.6 and from the Table 5.6, it is noticed that the proposed MCGDET-SAFF obtained less power consumption than the others. From the above discussion and Table 5.6, it is concluded that the proposed MCGDET-SAFF design circuit is highly suitable for emerging low power and high-speed applications.

5.6 CONCLUSION

From the overall experimental results and discussion given above, some of the suggestions are given here. The proposed MCGDET-SAFF is not designed directly from the basic Flip Flop design circuit. To obtain the final circuit with high efficiency in terms of low power and high speed, a stage wise improvement / modification is done on the edge triggered Flip Flop. For example, a sense amplified Flip Flop is incorporated with the clock gating for reducing the power consumption and reducing the memory. Then it will be extended into dual edge triggered clock gated sense amplifier Flip Flop. Finally, the CGDTSAFF is modified into MCGDET-SAFF and it can provide very less power consumption and it will increase the speed in the application.

The proposed MCGDET-SAFF comprises of CG circuit in the pulse generator design which acquires more delay in the Clk-to-Q and D-to-Q mechanism in MCGDET-SAFF. The proposed MCGDET-SAFF circuit obtained 79% less delay than existing architectures. The proposed design obtained substantial power reduction by integrating DET and conditional pre-charging. It also diminishes latency by using a fast latch. This new design is established to decrease the power dissipation and delay when associated with the clock gated sense amplifier Flip-Flop up to 26.1% and 86.5% respectively.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 CONCLUSION

A novel Flip-Flop framework for limited-power and elevated-performance is the main goal of this project. To do this, the study suggested on the dual edge triggered sense amplifier Flip-Flop, which utilizes several important characteristics, incorporated from multiple kinds of Flip-Flops. The primary characteristics used by several FFs are low energy consumption, less zone use, a decrease in energy leakage and a decrease in duration.

The suggested MCGDET-SAFF is derived from the modification or extension of the Flip Flop models. For example, from simple Flip Flop into sense amplified Flip Flop, the sense amplified Flip Flop into dual edge triggered Flip Flop, then it will be extended into clock gated dual edge triggered sense amplified Flip Flop. Finally, it is modified into MCGDET-SAFF. From the basic design each modification provides an improvement in decreasing power consumption and increasing the speed of the application where MCGDET-SAFF is used.

The proposed MCGDET-SAFF comprises of CG circuit in the pulse generator design which acquires more delay in the Clk-to-Q and D-to-Q mechanism in MCGDET-SAFF. The proposed MCGDET-SAFF circuit obtained 79% less delay than existing architectures. The proposed design obtained substantial power reduction by integrating DET and conditional pre-charging. It also diminishes latency by using a fast latch. This new design is established

to decrease the power dissipation and delay when associated with the clock gated sense amplifier Flip-Flop up to 26.1% and 86.5% respectively.

To lower the propagation delay period, two various types of DETFFs were suggested in this work. The recommended 1 Device uses a pass transistor for its data transfer and the recommended 2 device utilizes a transmission gate for the transferring of data to its output end. An extra inverter is fabricated in the later one for the transmission which results in increased layout area and more power consumption.

The recommended 1- DETFF works faster than the conventional DETFF with equal power utilization. So that, overall delay time has been reduced. In case of recommended 2 -DETFF consumes more power than the previous one. In the view of propagation Delay Product (PDP), at the supply voltage of 1.5V, the Recommended 1 model will surpass the traditional model by 29% and the recommended 2 will do the same by 12%.

A unique method, conditional discharge, is implemented to decrease shifting behaviour in Flip Flops of some inner nodes. This method was used in a double-edge continuous analog Flip-Flop, flexible clocking effect amplifier, Flip-Flop with conditional discharge. This research used multi threshold technology which is used to decrease energy again and the contrast between standard energy.

Finally, the proposed MCGDET-SAFF comprises of CG circuit in the pulse generator design which acquires more delay in the Clk-to-Q and D-to-Q mechanism in MCGDET-SAFF. The proposed MCGDET-SAFF circuit obtained 79% less delay than existing architectures. The proposed design obtained substantial power reduction by integrating DET and conditional pre-charging. It also diminishes latency by using a fast latch. This new design

is established to decrease the power dissipation and delay when associated with the clock gated sense amplifier flip-flop up to 26.1% and 86.5% respectively.

6.2 FUTURE WORK

In future, the proposed MCGDET-SAFF circuit can be experimented in various stages of design such as simple FF, SETFF, DETFF, SAFF, DETSAFF and CGDETSAFF by comparing the performance. Also, MCGDET-SAFF is directly used in various emerging applications and the results can be verified.

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LIST OF PUBLICATIONS

International Journals

1. **Mahendrakan, K** & Marimuthu, CN 2019, 'Design and Experiment A Modified Clock Gated Dual Edge Triggered Sense Amplified Flip Flops for Low Power and High-Performance Applications', Journal of Electrical Engineering, vol. 19, Issue no. 4, pp. 88-96 (**Impact Factor : 5.7840).**